

600V Half Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- $I_{\text{O+/-}}$ 4 A / 4 A
- V_{OUT} 7 V - 22 V
- $t_{\text{on/off}}$ (typ.) 170ns / 170ns

GENERAL DESCRIPTION

The SiLM22868 is a high voltage, high speed power MOSFET and IGBT drivers with high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to 600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 7 V to 22 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V and 15 V logic compatible
- Cross-conduction prevention logic
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT

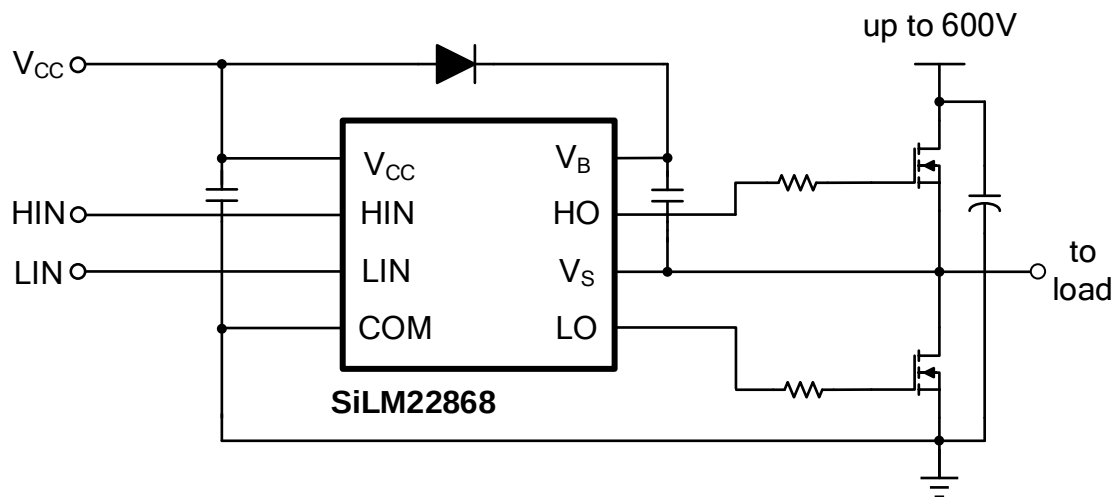


Figure 1. Typical Application Circuit

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PIN CONFIGURATION

Package	Pin Configuration (Top View)			
SOP8	1	V _{CC}	V _B	8
	2	HIN	HO	7
	3	LIN	V _S	6
	4	COM	LO	5

PIN DESCRIPTION

No.	Pin	Description
1	V _{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V _S	High-side floating supply return
7	HO	High-side gate drive output
8	V _B	High-side floating supply

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SiLM22868CA-DG	SOP8, Pb-Free	2500/Reel

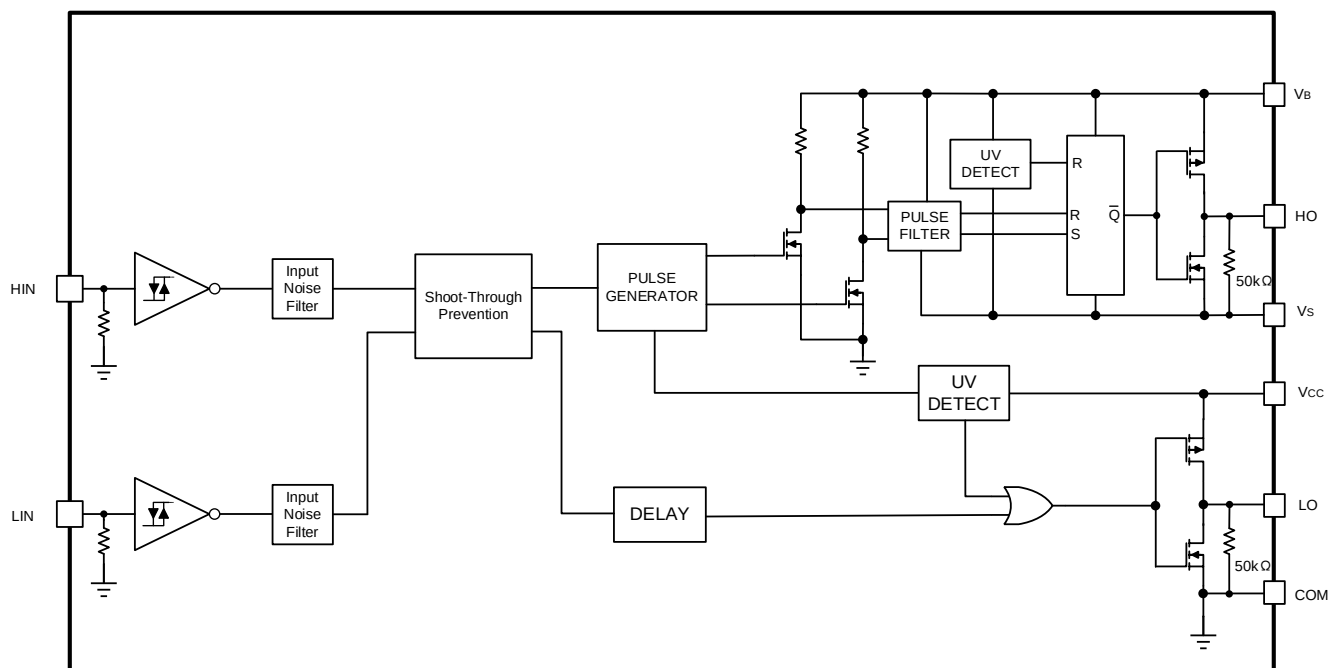
FUNCTIONAL BLOCK DIAGRAM


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	-0.3	650	V
V _S	High-side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High-side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V _{LO}	Low-side output voltage	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN & LIN)	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable offset supply voltage transient	---	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	---	0.625	W
θ _{JA}	Thermal resistance, junction to ambient	---	200	°C/W
T _J	Junction temperature	---	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	V _S + 7	V _S + 22	V
V _S	High-side floating supply offset voltage	-5	600	
V _{HO}	High-side floating output voltage	V _S	V _B	
V _{CC}	Low-side and logic fixed supply voltage	7	22	
V _{LO}	Low-side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN & LIN)	0	V _{CC}	
T _A	Ambient temperature	- 40	125	°C

Note: For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0\text{ V}$	---	170	250	ns
t_{off}	Turn-off propagation delay	$V_S = 0\text{ V}$	---	170	250	
t_r	Turn-on rise time		---	9	15	
t_f	Turn-off fall time		---	9	15	
MT	Delay matching, HS & LS turn-on/off		---	---	35	

STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage threshold	$I_O = 20\text{ mA}$	1.6	2.0	2.5	V
V_{IL}	Logic "0" input voltage threshold		0.8	1.2	1.5	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$		---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.03	0.15	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V}$	20	50	80	
I_{QCC}	Quiescent V_{CC} supply current		80	170	260	
I_{IN+}	Logic "1" input bias current	$HIN=LIN = 5\text{ V}$	---	25	35	
I_{IN-}	Logic "0" input bias current	$HIN=LIN = 0\text{ V}$	---	---	5	
V_{CCUV+}, V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold		5.65	6.25	6.85	V
V_{CCUV-}, V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold		4.95	5.55	6.15	
I_{O+}	Output high short circuit pulsed current ¹	$V_O = 0\text{ V}$, $V_{IN} = \text{Logic "1"}$	---	4.0	---	A
I_{O-}	Output low short circuit pulsed current ¹	$V_O = 15\text{ V}$, $V_{IN} = \text{Logic "0"}$	---	4.0	---	

(1) Values are verified by characterization on bench.

SWITCHING AND TIMING RELATIONSHIPS

The relationships between the input and output signals of the SiLM22868 are illustrated below in Figure 3, Figure 4, Figure 5.. These figures show the definitions of several timing parameters (i.e., t_{on} , t_{off} , t_r , and t_f) associated with this device.

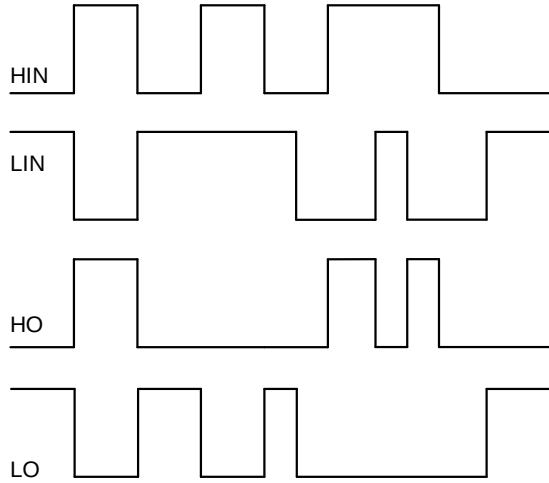


Figure 3. Input/Output Timing Diagram

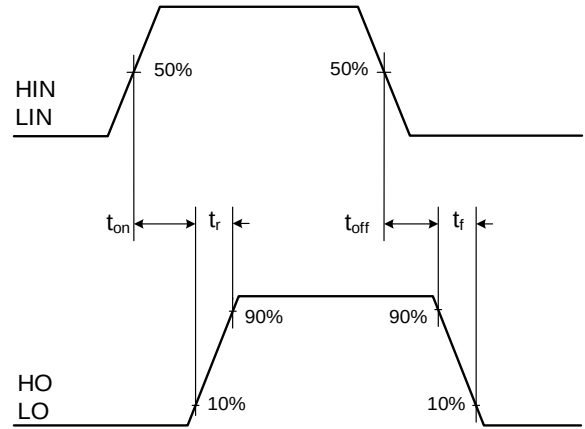


Figure 4. Switching Time Waveform

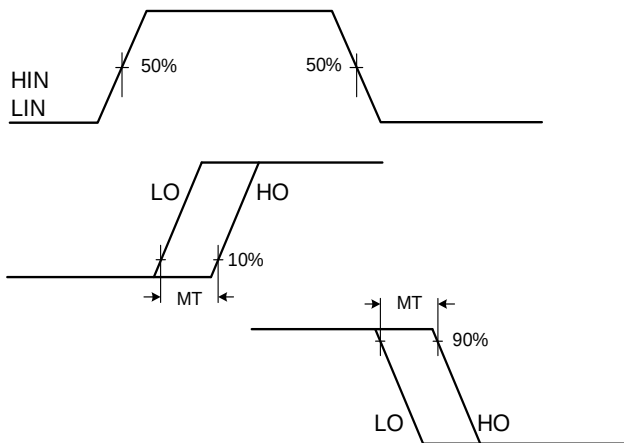


Figure 5. Delay Matching Waveform

PACKAGE CASE OUTLINES

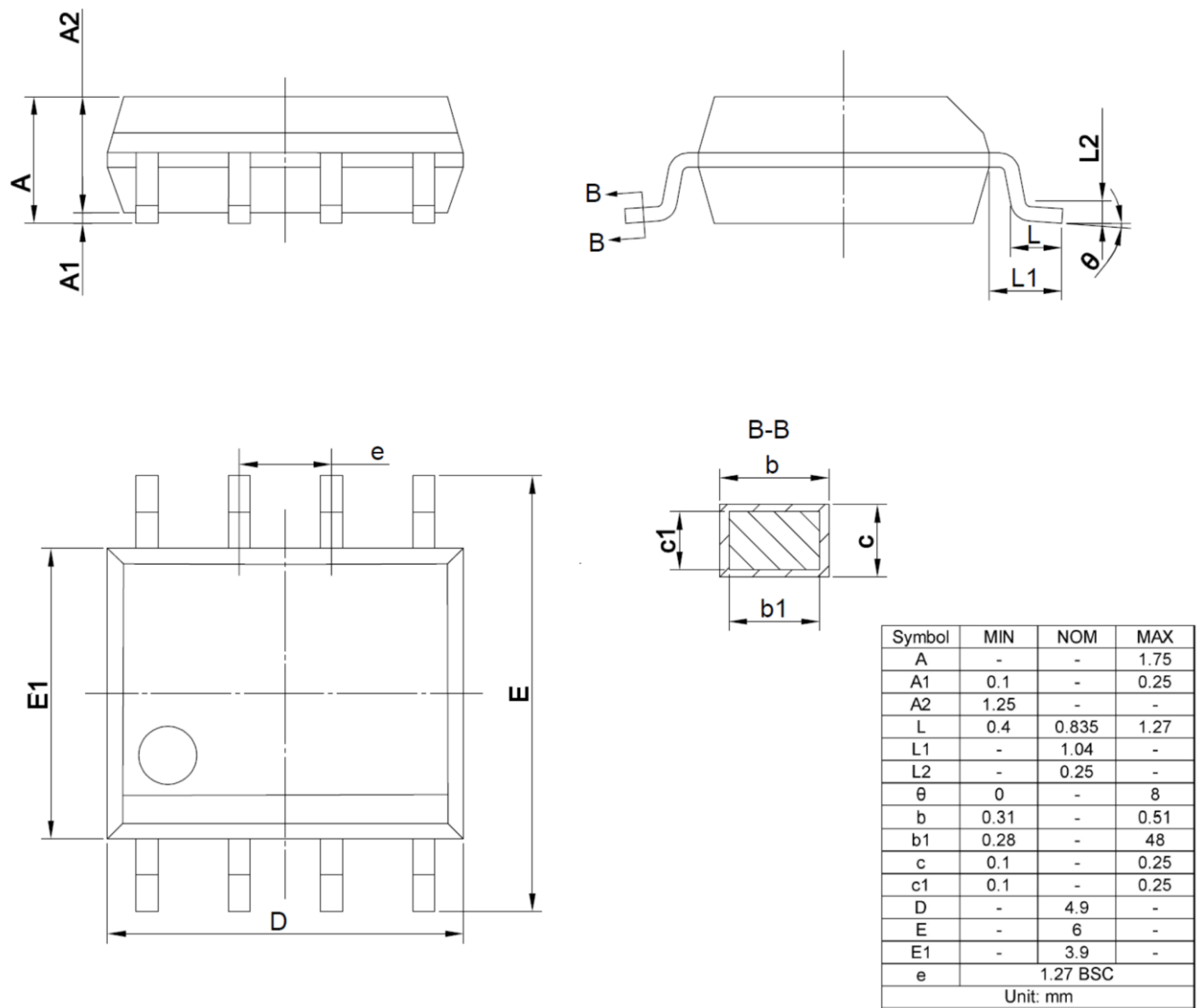


Figure 6. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2025-07-06	
Whole document	Initial datasheet release.
Rev 1.1 datasheet, 2025-12-06	
Page 6	Update EC table.