Low-Voltage H-Bridge Driver

GENERAL DESCRIPTION

The SLM8837 device provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one DC motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The SLM8837 device can supply up to 1.8 A of output current. It operates on a motor power supply voltage from 0 to 11 V, and a device power supply voltage of 1.8 V to 5.5 V.

The SLM8837 device has a PWM (IN1 and IN2) input interface. Both interfaces are compatible with industry-standard devices.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, under-voltage lockout, and over-temperature.

FEATURES

- H-Bridge Motor Driver
  - Drives a DC Motor or Other Loads
  - Low On-Resistance: HS + LS 280 mΩ
- 1.8A Maximum Drive Current
- Separate Motor and Logic Supply Pins
  - Motor VM: 0 to 11 V
  - Logic VCC: 1.8 to 5.5 V
- PWM Interface
  - PWM, IN1 and IN2
- Low Power Sleep Mode with Total 120nA Maximum Sleep Current
- Small Package and Footprint
  - 8 Pin DFN8 With Thermal Pad
  - 2.0 mm × 2.0 mm
- Protection Features
  - VCC Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

APPLICATIONS

- Consumer Products
- Toys
- Cameras
- Medical Devices

TYPICAL APPLICATION CIRCUIT

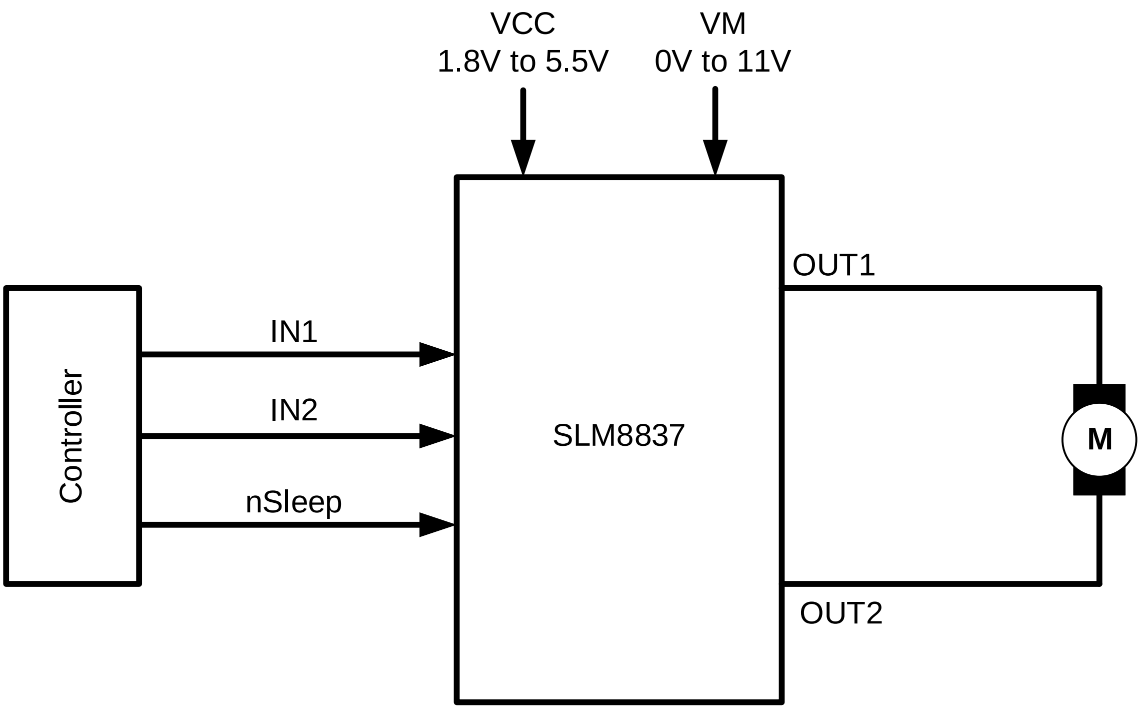

Figure 1. SLM8837 application circuit

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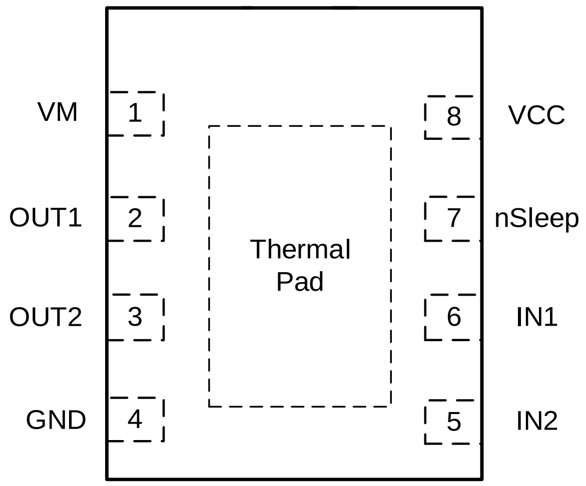
PIN CONFIGURATION

Package	Pin Configuration (Top View)
DFN8	

PIN FUNCTION DESCRIPTIONS

No.	Pin Name	Function Description
1	VM	Motor power supply Bypass this pin to the GND pin with a 0.1µF ceramic capacitor rated for VM.
2	OUT1	Motor output
3	OUT2	Connect these pins to the motor winding.
4	GND	Device ground This pin must be connected to ground.
5	IN2	IN2 input See the Detailed Description section for more information
6	IN1	IN1 input See the Detailed Description section for more information
7	nSLEEP	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown.
8	VCC	Logic power supply Bypass this pin to the GND pin with a 0.1µF ceramic capacitor rated for VCC.
	Exposed Pad	Connect the exposed pad to an external ground plane to improve thermal performance.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM8837EF-7G	DFN2x2-8L	3000/Reel

FUNCTIONAL BLOCK DIAGRAM

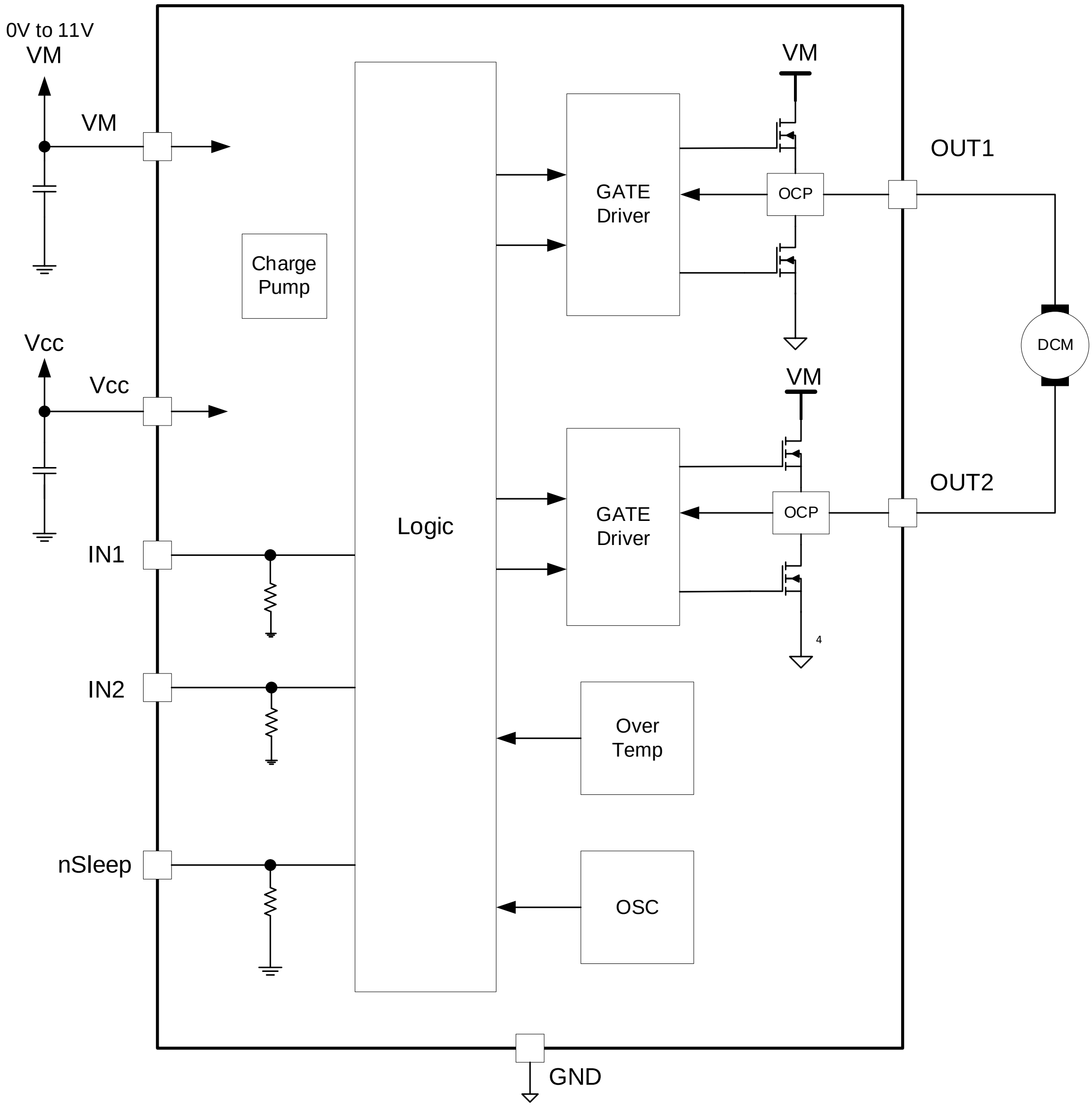


Figure 2. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
VM, Motor power-supply voltage	-0.3V to +12V
VCC, Logic power-supply voltage	-0.3V to +6V
IN1, IN2, nSLEEP, Control pin voltage	-0.5V to +6V
Operation Junction temperature, T_J	-40°C to 150°C
Storage temperature, T_S	-60°C to 150°C

Note:
Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. All voltage parameters are absolute voltages referenced to GND. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

QUALIFICATION RATINGS

Symbol	Description	Value	Unit
V_{ESD}	HBM	±2500	V
	CDM	±1500	V

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
VM	Motor power-supply voltage		11	V
VCC	Logic power supply voltage	1.8	5.5	V
I_{OUT}	Output peak current		1.8	A
F_{PWM}	Externally applied PWM frequency		250	kHz
V_{LOGIC}	Logic level input voltage		5.5	V
T_A	Operation ambient temperature	-40	85	°C

Note: Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

Over operating free-air temperature range (unless otherwise noted)

Symbol	Definition	Thermal resistance	Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over recommended operating conditions unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES (VM, VCC)						
VM	VM operating voltage				11	V
I_{VM}	VM operating supply current	VM = 5 V; VCC = 3 V; No PWM			1	μA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		65		μA
I_{VMQ}	VM sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		20		nA
VCC	VCC operating voltage		1.8		5.5	V
I_{VCC}	VCC operating supply current	VM = 5 V; VCC = 3 V; No PWM		1.15	1.35	mA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		1.2	1.4	mA
I_{VCCQ}	VCC sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		5	200	nA
CONTROL INPUTS (IN1, IN2, nSLEEP)						
V_{IL}	Input logic-low voltage falling threshold		0.25 × VCC	0.38 × VCC		V
V_{IH}	Input logic-high voltage rising threshold			0.46 × VCC	0.5 × VCC	V
V_{HYS}	Input logic hysteresis			0.08 × VCC		V
I_{IL}	Input logic low current	V_{IN} = 0 V	-5		5	μA
I_{IH}	Input logic high current	V_{IN} = 3.3 V			50	μA
		V_{IN} = 3.3 V		35	50	μA
R_{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(on)}$	HS + LS FET on-resistance	VM = 5 V; VCC = 3 V; I_O = 800 mA; T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = 0 V	-200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{DEG}	Overcurrent deglitch time			1		μs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD}	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

TIMING REQUIREMENTS

T_A = 25°C, VM = 5 V, VCC = 3 V, RL = 20 Ω, detail time definition see Figure 3.

Symbol	Definition	Min	Max	Units
t_7	Output enable time[1]		300	ns
t_8	Output disable time[1]		300	ns
t_9	Delay time, INx high to OUTx high[1]		200	ns
t_{10}	Delay time, INx low to OUTx low[1]		200	ns
t_{11}	Output rise time[1]		188	ns
t_{12}	Output fall time[1]		188	ns
t_{wake}	Wake time, nSLEEP rising edge to part active[1]		30	us

1) Values are verified by characterization on bench

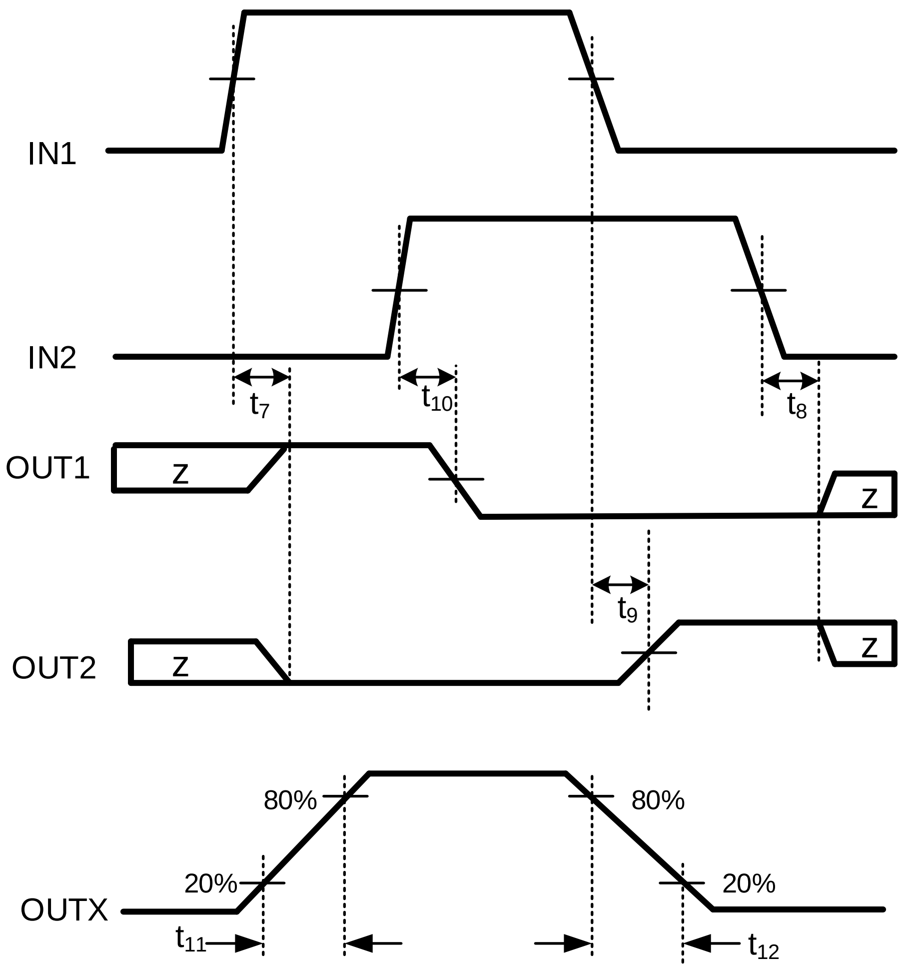


Figure 3. Input and Output Timing for SLM8837

FUNCTION DESCRIPTION

Overview

The SLM8837 is an H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using a PWM interface (IN1 and IN2) on the SLM8837 device. A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

The SLM8837 greatly reduces the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the SLM8837 adds protection features beyond traditional discrete implementations: under-voltage lockout, over-current protection, and thermal shutdown.

Bridge Control

The SLM8837 device is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin. Table 1 shows the logic for the SLM8837 device.

Table 1. SLM8837 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the SLM8837 enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 5.5 V.

The VM voltage supply does not have any under-voltage lockout protection (UVLO), so as long as VCC > 1.8 V, the internal device logic remains active, which means that the VM pin voltage can drop to 0 V. However, the load cannot be sufficiently driven at low VM voltages.

Protection Circuits

The SLM8837 device is fully protected against VCC under-voltage, over-current, and over-temperature events.

VCC Undervoltage Lockout

If at any time the voltage on the VCC pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent Protection

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Over-current conditions are detected on both the high-side and low-side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

Thermal Shutdown

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 2. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I_{OUT} > 1.9 A (MIN)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J > 150°C (MIN)	Disabled	T_J < 150°C

Device Functional Modes

The SLM8837 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The SLM8837 is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during under-voltage lockout, over-current, and over-temperature fault conditions.

Table 3. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

APPLICATION AND IMPLEMENTATION

Application Information

The SLM8837 is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the SLM8837 device.

Typical Application

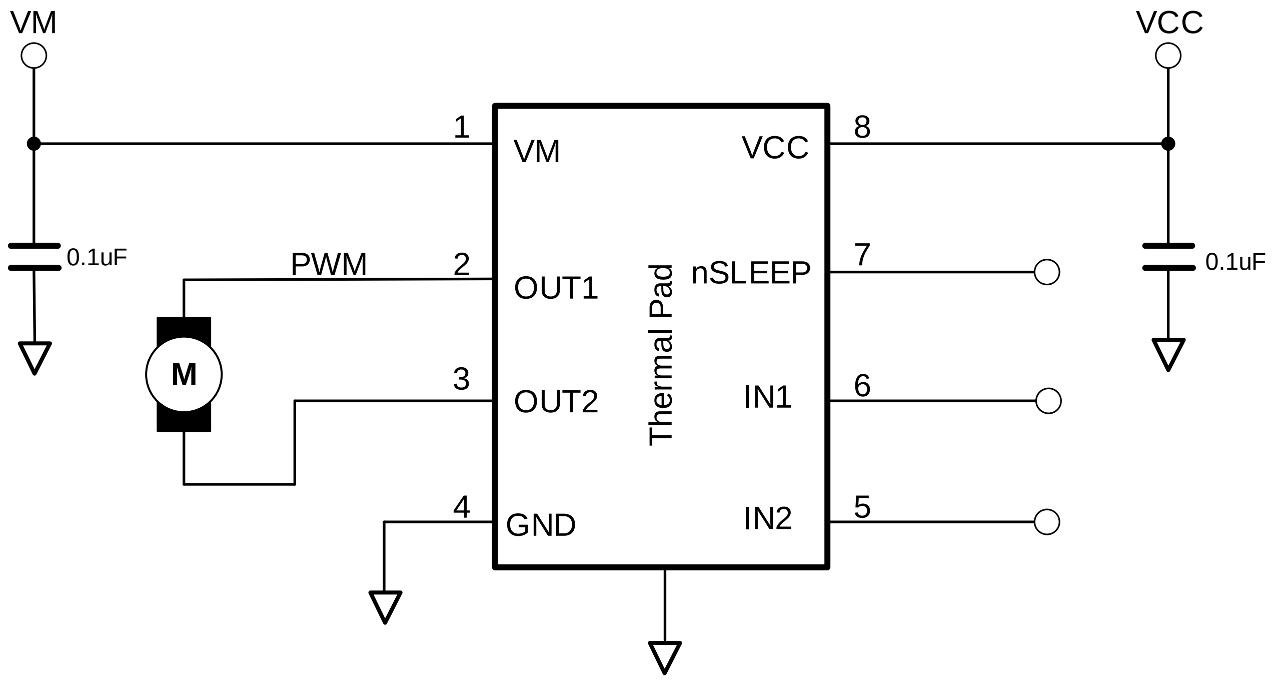


Figure 4. SLM8837 Application Circuit

Design Requirements

Table 4 lists the required parameters for a typical usage case.

Table 4. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target rms current	I_{OUT}	0.8 A

Detailed Design Procedure

Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

Low-Power Operation

When entering sleep mode, it is recommended to set all inputs as a logic low to minimize system power.

Power Supply Recommendations

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripples
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

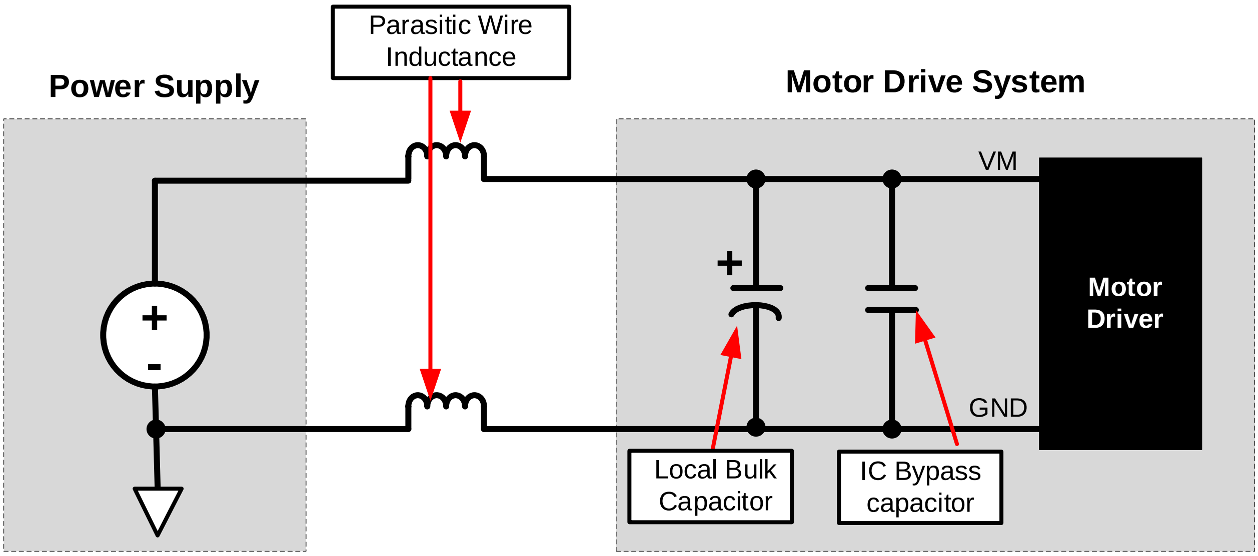


Figure 5. Example Setup of Motor Drive System with External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

Layout Guidelines
The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

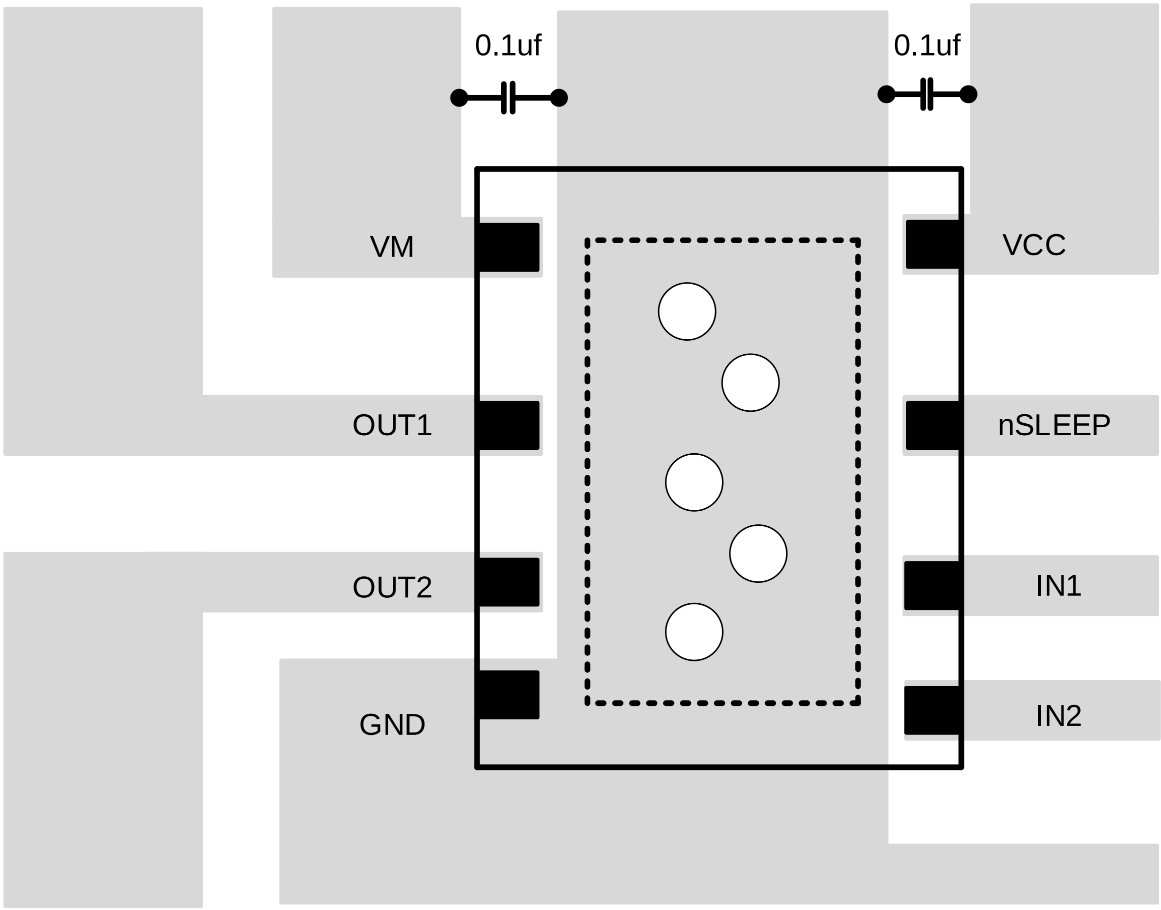


Figure 6. Simplified Layout Example

Power Dissipation
Power dissipation in the SLM8837 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Use below equation to estimate the average power dissipation when running a stepper motor.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

Where

- P_{TOT} is the total power dissipation
- $R_{DS(on)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the rms or dc output current being supplied to the load

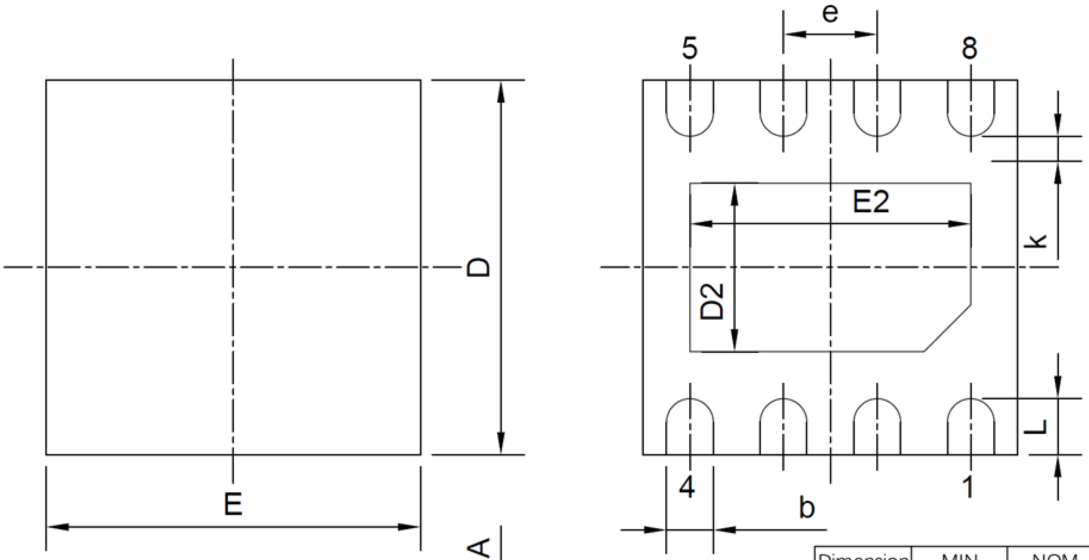
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

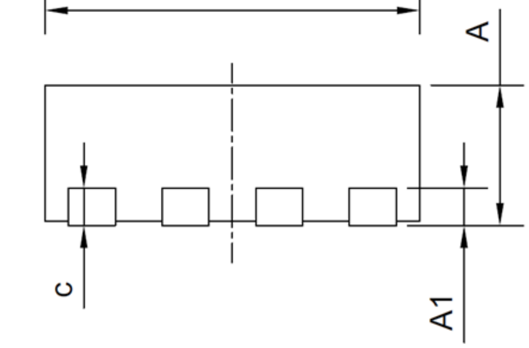
The value of $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases.

SLM8837 has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high ambient temperature.

PACKAGE CASE OUTLINES





Dimension	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
c		0.203REF	
D	1.9	2	2.1
E	1.9	2	2.1
D2	0.8	0.9	1
E2	1.45	1.5	1.55
b	0.2	0.25	0.3
e	0.4	.0.5	0.6
L	0.25	0.3	0.35
k	0.15	0.25	0.35
Unit : mm			

Figure 7. DFN2×2-8L Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 Datasheet: 2024-07-23	
Whole document	Initial datasheet