High Efficiency, 95V, 0.5A Synchronous Step Down Regulator

GENERAL DESCRIPTION

The SiLM6582/83 is a high efficiency synchronous step down regulator. It can deliver 0.5 A continuous current. The SiLM6582/83 operates over a wide input voltage range from 6V to 95V and integrates the main switch and synchronous switch with very low R_{DSON} to minimize the power loss and provide a high efficiency solution.

The SiLM6582/83 adopts the constant on time (COT) control architecture to achieve fast transient response. The ultra-low quiescent and diode emulation mode operation improves the efficiency at light load.

The SiLM6582/83 provides internal soft start to limit inrush current. The programmable UVLO pin provide a flexible way to program the startup input voltage and an open drain power good output to indicate the health of the regulator. It also integrates peak and valley current limit protection, thermal shutdown protection.

The SiLM6582/83 operates over −40°C to +150°C junction temperature range and is available in SOP8-EP package.

FEATURES

- Wide input voltage range: 6V to 95V
- Output current capability: 0.5 A
- 1.2V reference voltage with ±1.5% accuracy over temperature
- Integrates low R_{DSON} high side/ low side FET: 600mΩ/290 mΩ
- 20μA quiescent current and 15μA shutdown current
- Constant on time control for fast transient response
- Integrates soft start to limit inrush current
- Open drain power good output
- Programmable UVLO
- Peak and valley current limit protection
- Thermal shutdown protection
- Compact package: SOP8-EP

APPLICATIONS

- Telecom supplies
- High-cell-count battery packs (E-bike, E-Scooter)
- Motor drives, drones
- High voltage post regulator

TYPICAL APPLICATION CIRCUIT

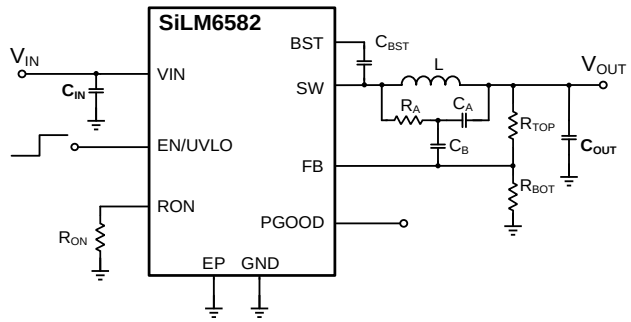

Figure 1. SiLM6582 Application Circuit

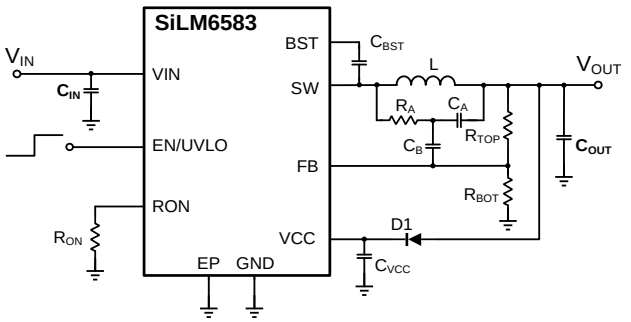

Figure 2 SiLM6583 Application Circuit

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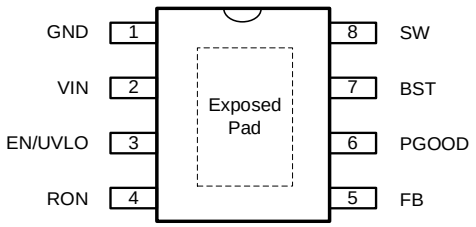
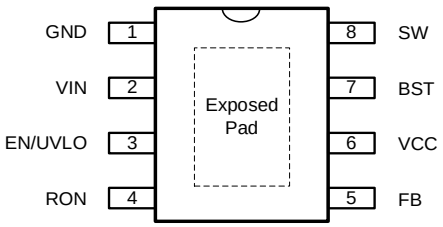
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8-EP	 SiLM6582  SiLM6583

PIN FUNCTION DESCRIPTIONS

No.	Pin Name	Function Description
1	GND	Ground for internal circuits.
2	VIN	Power supply input. Connect a bypass capacitor between this pin and GND.
3	EN/UVLO	Precision enable input and under-voltage lockout(UVLO) programming pin. An external resistor divider can be used to program the UVLO threshold. If the enable pin is not used, connect this pin to VIN.
4	RON	On-time programming pin. Connect a resistor between this pin and GND to set the high side switch on-time.
5	FB	Feedback voltage sense input. Connect this pin to a resistor divider from the output voltage.
6	PGOOD	PGOOD (SiLM6582): Power good output (Open Drain). Connect this pin to a power supply through an external pull-up resistor between 10kΩ to 100kΩ.
	VCC	VCC (SiLM6583): Internal 5 V LDO output or input voltage for the control circuit. Place a 1 µF ceramic capacitor between VCC and GND.
7	BST	Bootstrap gate-drive supply. Required to connect a 3.3 nF 50V X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	Switching node. Connect to the switching node of the power inductor.
	Exposed Pad	Connect the exposed pad to an external ground plane to improve thermal performance.

ORDERING INFORMATION

Order Part No.	Pin 6 Function	Package	QTY
SiLM6582CB-DG	PGOOD	SOP8-EP	2500/Reel
SiLM6583CB-DG	VCC	SOP8-EP	2500/Reel

FUNCTIONAL BLOCK DIAGRAM

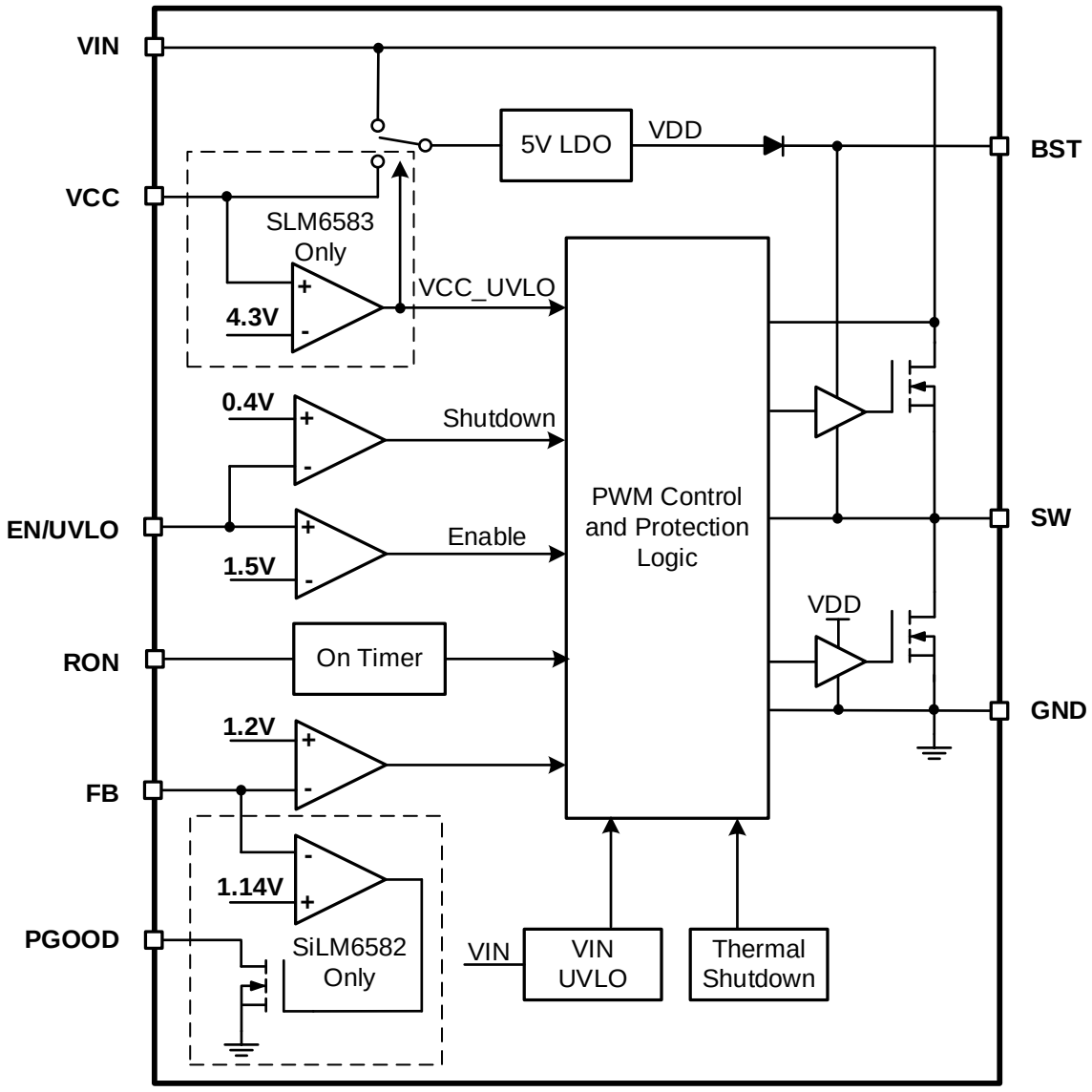


Figure 3. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
VIN, EN/UVLO	-0.3V to +100V
SW	-0.3V to +100V
BST	V_{SW}+6V
RON, FB	-0.3V to +6V
VCC, PGOOD	-0.3V to +30V
External capacitance between BST and SW	2.3 nF to 4.0 nF
Thermal resistance, SOP8-EP, Junction to ambient, θ_{JA}	41°C/W
Operation Junction temperature, T_J	-40°C to 150°C
Storage temperature, T_S	-55°C to 150°C

Note:
Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. All voltage parameters are absolute voltages referenced to GND. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Nom	Max	Units
V_{IN}	Input voltage	6		95	V
I_{OUT}	Output current		0.5		A
t_{ON}	On time	0.1		10	μs
f_{SW}	Operation switching frequency			500	kHz
C_{BST}	Capacitance between BST and SW		3.3		nF
T_J	Junction temperature	-40		150	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 5.0V, T_J = 25°C for typical specifications and T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN Power Supply						
V_{VIN}	Input voltage range on VIN		6		95	V
I_{VIN_ACTIVE}	Active current on VIN	V_{EN} = 2.5V		700	900	μA
I_{VIN_SLEEP}	Sleep current on VIN	V_{FB} = 1.5V, V_{EN} = 2.5V		20	35	μA
I_{VIN_SD}	Shutdown current on VIN	V_{EN} = GND		15	30	μA
V_{UVLO}	Under voltage lockout threshold	V_{VIN} rising	4.7	5.2	5.7	V
V_{UVLO_HYS}	Under voltage lockout hysteresis			200		mV
VCC Power Supply (SiLM6583 only)						
V_{VCC}	Voltage range on VCC		4.5		30	V
$V_{VCC\_UVLO\_R}$	Under voltage lockout threshold	V_{VCC} rising		4.3		V
$V_{VCC\_UVLO\_F}$	Under voltage lockout threshold	V_{VCC} falling		4.05		V
Feedback Voltage						
V_{FB}	Feedback reference voltage		1.182	1.2	1.218	V
EN/UVLO						
$V_{EN\_SHDN\_R}$	EN shutdown rising threshold				1.1	V
$V_{EN\_SHDN\_F}$	EN shutdown falling threshold		0.4			V
V_{EN_R}	EN enable rising threshold		1.44	1.52	1.6	V
V_{EN_HYS}	EN enable hysteresis			100		mV
Bootstrap Voltage						
$V_{BST\_UVLO\_R}$	V_{BST} UVLO threshold rising		2.2	2.7	3.2	V
$V_{BST\_UVLO\_F}$	V_{BST} UVLO threshold falling		2.0	2.5	3.0	V
Power MOSFET						
R_{DSON_HS}	High side MOSFET ON Resistance	I_{SW} = 0.1 A		600		mΩ
R_{DSON_LS}	Low side MOSFET ON Resistance	I_{SW} = -0.1 A		290		mΩ
Current Limit						
$I_{LIM\_HS\_PK}$	High side peak current limit		0.65	0.82		A
$I_{LIM\_LS\_PK}$	Low side peak current limit		0.65	0.82		A
$I_{LIM\_LS\_VL}$	Low side valley current limit		0.5	0.65	0.78	A
Soft Start						
t_{SS}	Soft start time		2	3	4	ms

Timing						
t_{MIN_OFF}	Minimum off time			200		ns
t_{ON}	On time	V_{VIN} = 48V, R_{ON} = 100 kΩ		833		ns
Power Good (SiLM6582 only)						
V_{PG_R}	Power good rising threshold		1.09	1.14	1.18	V
V_{PG_F}	Power good falling threshold		1.03	1.08	1.12	V
R_{PG}	Pull down resistance on PGOOD	V_{FB} = 1V, IPG = 1mA		30		Ω
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown Threshold			175		°C
T_{SHDN_HYS}	Thermal Shutdown Hysteresis			15		°C

TYPICAL PERFORMANCE CHARACTERISTICS

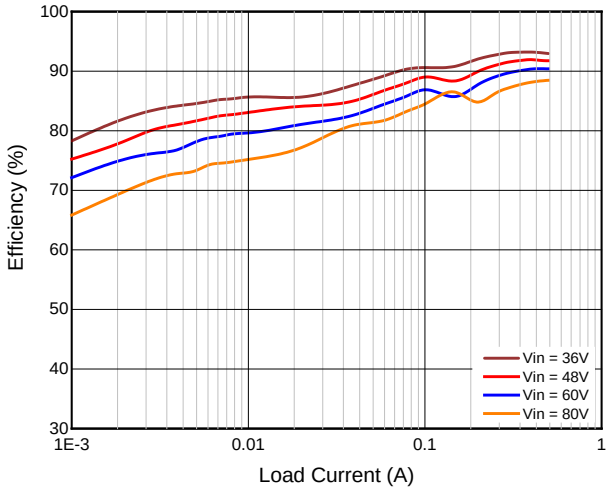


Figure 4. Power Conversion Efficiency(Log Scale)
VOUT=12V

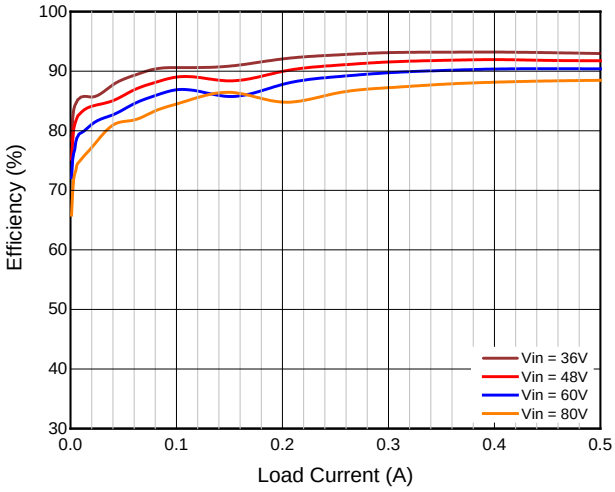


Figure 5. Power Conversion Efficiency(Linear Scale)
VOUT=12V

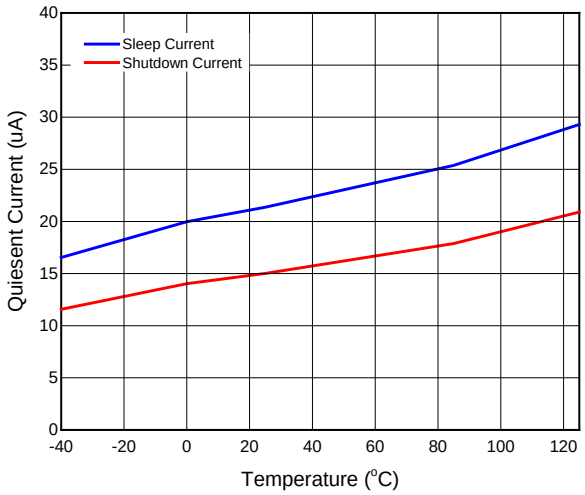


Figure 6. Quiescent Current vs. Temperature
VIN=48V

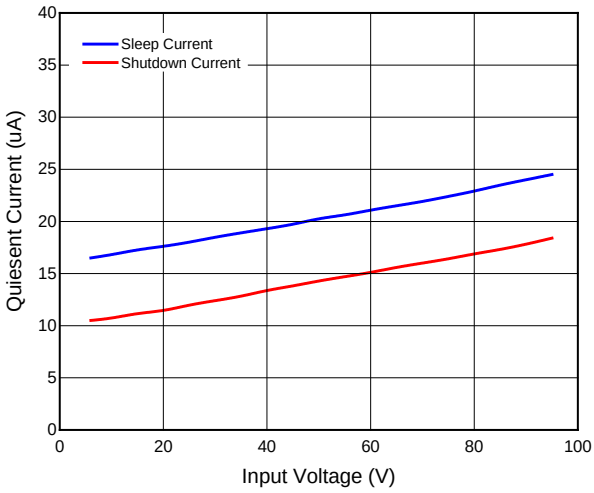


Figure 7. Quiescent Current vs. Input Voltage

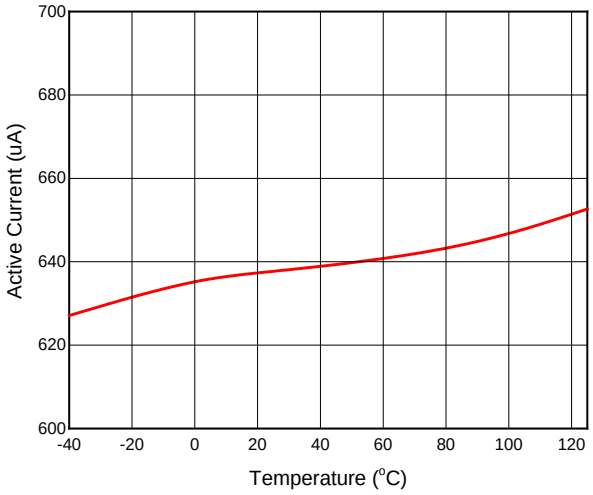


Figure 8. Active Current vs. Temperature
VIN=48V

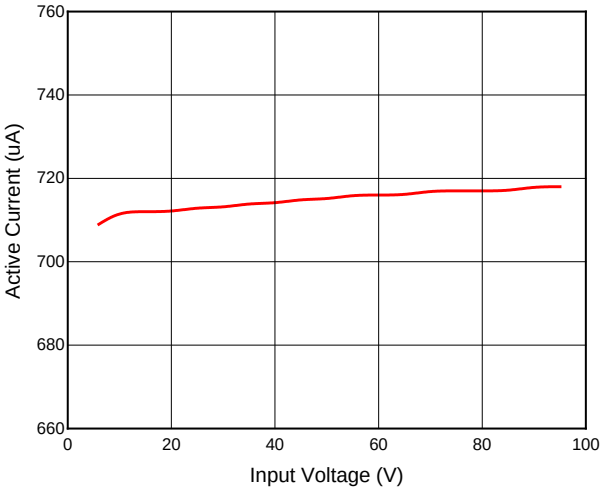


Figure 9. Active Current vs. Input Voltage

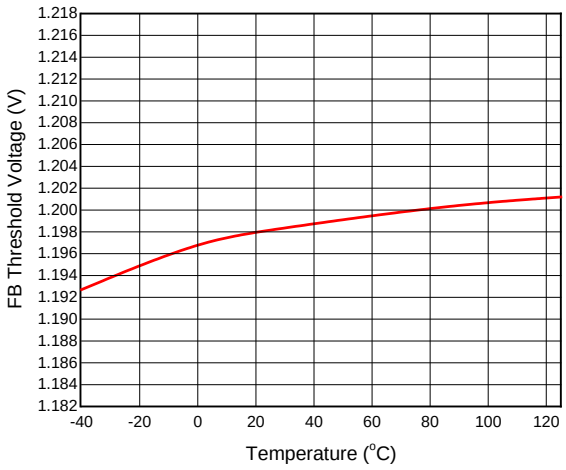


Figure 10. FB Threshold Voltage vs. Temperature

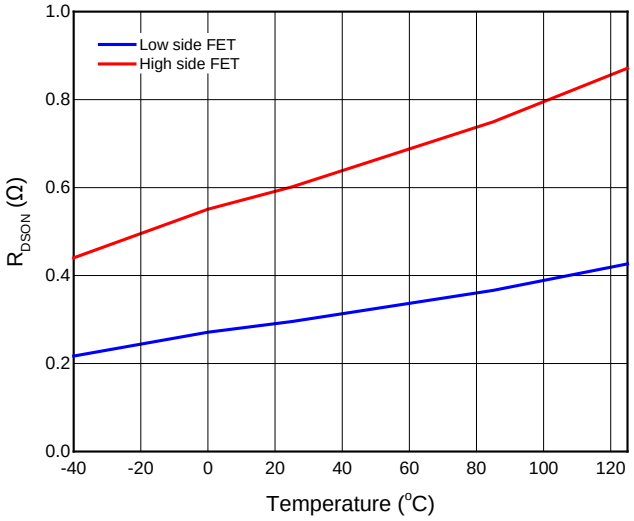


Figure 11. High side and Low side R_{DSON} vs. Temperature

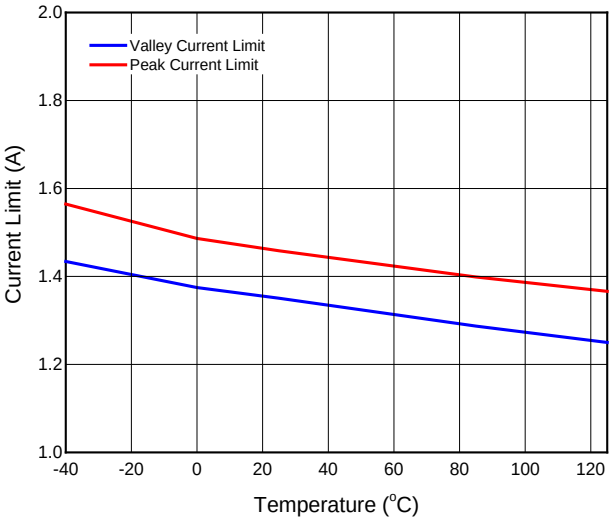


Figure 12. Peak and Valley Current Limit vs. Temperature

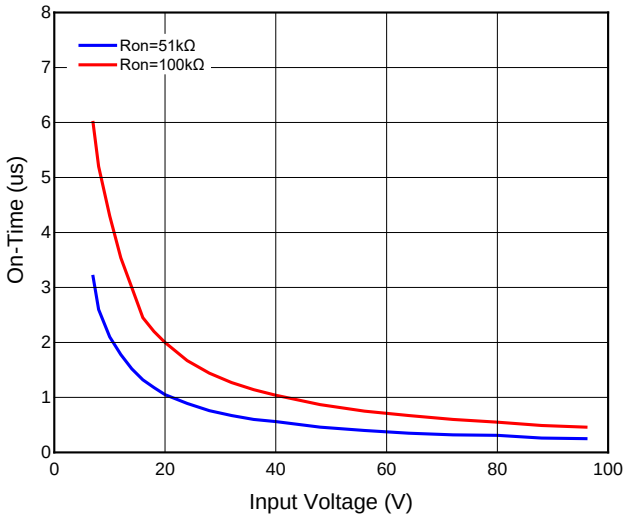


Figure 13. COT On-Time vs. Input Voltage

FUNCTION DESCRIPTION

Control Scheme

The SiLM6582/83 adopts a constant on time (COT) control scheme. The COT control scheme sets a fixed on-time t_{ON} of the high-side MOSFET using a timing resistor (R_{ON}). The t_{ON} is adjusted as input voltage changes and is inversely proportion to input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON}, the high side MOSFET turns off until the feedback pin is equal or below the reference voltage of 1.2 V. In order to maintain stability, the feedback comparator requires a minimal ripple voltage that is in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage during the off-time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 50 mV. Refer to **Ripple Injection** section to ensure stability over the full input voltage range with different configuration.

Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains highest efficiency at light load currents by decreasing the effective switching frequency. DEM operation occurs when the low side MOSFET off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. Power conversion efficiency is thus higher in a DEM regulator than an equivalent forced-PWM CCM regulator. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases. When this idle duration exceeds 15 μs, the regulator transitions into an ultra-low I_Q mode, consuming only 15 μA quiescent current from the input.

Output Voltage Setting

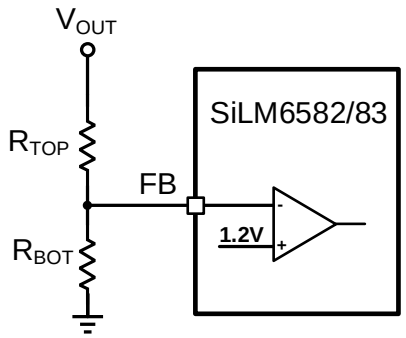


Figure 14. Output Voltage Setting

The SiLM6582/83 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage. The output voltage is setting by an external resistor divider.

$$V_{OUT}=1.2\times(1+\frac{R_{TOP}}{R_{BOT}})$$

ON-Timer Setting

The on-time of the SiLM6582/83 is determined by the resistance between the RON and ground (R_{ON}), and is inversely proportional to the input voltage, V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied.

The on time can be calculated using the below equation:

$$t_{ON}(\mu s)=\frac{R_{ON}\ (k\Omega)}{2.5\times V_{IN}}$$

The R_{ON} can be calculated by the below equation:

$$R_{ON}(k\Omega)=\frac{2500\times V_{OUT}}{f_{SW}(kHz)}$$

t_{ON}: the on time of the high side switch.

V_{IN}: the input voltage.

R_{ON}: the resistance between the RON and ground.

V_{OUT}: the output voltage.

f_{SW}: the switching frequency.

Select R_{ON} for the on-time is greater than t_{MIN_ON} (50 ns) and is less than t_{MAX_ON} (10μs) over the input voltage for proper operation.

External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for internal high side MOSFET. A high quality 3.3nF 50V X7R ceramic capacitor is recommended to be placed between the BST and SW pin.

Output Inductor

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. As a guideline, the inductor ripple current, ΔI_L, is typically set to 1/3 of the maximum load current. The inductor value can be calculated using the following equation:

$$L=\frac{(V_{IN}-V_{OUT})\times D}{\Delta I_L \times f_{SW}}$$

where:

V_{IN} is the input voltage.

V_{OUT} is the output voltage.

ΔI_L is the inductor ripple current.

f_{SW} is the switching frequency.

D is the duty cycle.

The saturation current of the inductor must be larger than the peak current limit.

The rms current of the inductor should be greater than the value calculated by the following equation:

$$I_{RMS}=\sqrt{{I_{OUT}}^2+\frac{{\Delta I_L}^2}{12}}$$

Where:

I_{RMS} is the RMS current of the inductor.

I_{OUT} is the output current.

ΔI_L is the inductor ripple current.

Output Capacitor

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use an X5R or X7R ceramic capacitor, and capacitance value is greater than 10μF.

Input Capacitor

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. This capacitor should be a ceramic capacitor in the range of 10 μF to 47 μF and must be placed close to the VIN pin. The loop composed of this input capacitor, high-side MOSFET, and low-side MOSFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor should be larger than the following equation:

$$I_{RMS\_CIN}=I_{OUT}\times\sqrt{D\times(1-D)}$$

Where:

I_{RMS_CIN} is the RMS current on the input capacitor.

I_{OUT} is the output current.

D is the duty cycle.

Ripple Injection

The SiLM6582/83 adopts a COT control scheme and the PWM timing is based on the output voltage ripple feedback to the FB pin. Typically ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in-phase with the inductor current. This triangular wave is the AC-coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, it is suited for applications where low output voltage ripple is critical.

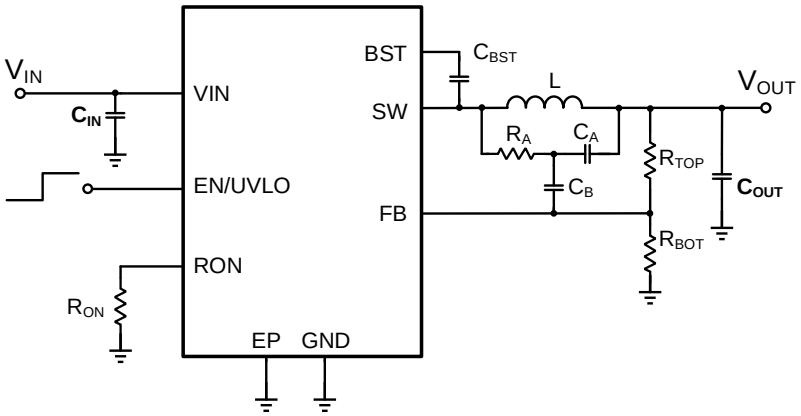


Figure 15. Ripple Generation Circuit

The R_A, C_A, C_B shall meet the below equations to make sure the system is stable.

$$C_A \geq \frac{10}{2\times\pi\times f_{sw}\times(R_{TOP}//R_{BOT})}$$

$$R_A \times C_A \leq \frac{V_{IN}\text{-}V_{OUT}}{50mV}\times t_{ON}$$

$$C_A \geq 4\times C_B$$

$$C_B \geq \frac{t_{TR}}{3\times R_{TOP}}$$

Here t_{TR} is the recovery time during the transient.

Table 1 lists several typical application cases which recommend the ripple feedback parameter selection.

Table 1. SiLM6582/83 Ripple Generation Parameter Recommendation

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	Inductor (uH)	C_{OUT} (uF)	R_{BOT}(kΩ)	R_{TOP}(kΩ)	R_A(kΩ)	C_A(pF)	C_B(pF)
12	5	300	33	44	49.9	158	240	820	160
24	5	300	33	44	49.9	158	330	820	160
48	5	300	33	44	49.9	158	360	820	160
24	12	300	68	44	49.9	449	120	3300	56
48	12	300	68	44	49.9	449	160	3300	56

Enable/Under-Voltage Lockout (EN/UVLO)

The SiLM6582/83 contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 1.1 V (typical), the regulator is in a low-current shutdown mode and the input current (I_{VIN_SD}) is dropped down to 15 μA. When the voltage is greater than 1.1 V but less than 1.5 V (typical), the regulator is in standby mode. In standby mode the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5 V (typical), normal operation begins.

The SiLM6582/83 also provides an UVLO programmable function. An external resistor divider from VIN to GND can be used to set the minimum operating voltage of the regulator as shown in Figure 16. Use below equation to calculate the input UVLO turn on and turn off voltages:

$$V_{IN\_ON}=1.5\times(1+\frac{R_{TOP\_EN}}{R_{BOT\_EN}})$$

$$V_{IN\_OFF}=1.4\times(1+\frac{R_{TOP\_EN}}{R_{BOT\_EN}})$$

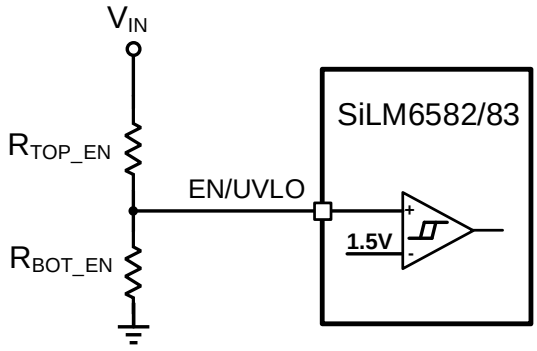


Figure 16. Input UVLO Threshold Program

If input UVLO is not required, the EN/UVLO pin can be used as an enable input driving by a logic signal or connecting it directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching as soon as the internal bias rails are active.

Internal Regulator

The SiLM6582 integrates an internal linear regulator (VDD) that is powered from VIN with a nominal output of 5 V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VDD regulator supplies current to internal circuit blocks including the synchronous FET driver and logic circuits.

The SiLM6583 has a VCC pin which provides another input to the internal VDD regulator. When the VCC voltage is larger than 4.3V, the power supply of internal VDD regulator is switched to VCC. This feature reduces power consumption on the VDD regulator like connecting the VCC to the output of the buck as shown in Figure 2.

Soft Start

The SiLM6582/83 integrates an internal soft-start circuit to control the output voltage ramps up gradually, thereby reducing inrush current during the start up. The soft-start time is internally set to 3 ms.

Current limit

The SiLM6582/83 integrates overcurrent protection with cycle-by-cycle current limiting of the peak inductor current. The high-side MOSFET current is sensed and compared every switching cycle to the peak current limit threshold.

To protect the regulator from potential current runaway conditions, the SiLM6582/83 includes a fold-back valley current limit feature that is enabled if a peak current limit is detected. As shown in Figure 17, if the peak current in the high-side MOSFET exceeds the peak current limit threshold (0.82 A typical), the present cycle is immediately terminated regardless of the programmed on-time (t_{ON}), the high-side MOSFET is turned off and the fold-back valley current limit is activated. The low-side MOSFET remains on until the inductor current drops below this fold-back valley current limit (0.65 A typical), after which the next on-pulse is initiated. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 0.5 A to ensure proper short-circuit and heavy-load protection of the SiLM6582/83.

Current is sensed after a leading-edge blanking time following the high-side MOSFET turn on transition. The propagation delay of the current limit comparator is 100 ns. During high step-down conditions when the on-time is less than 100 ns, a back-up peak current limit comparator in the low-side MOSFET also set at 0.82 A will enable the fold-back valley current limit set at 0.65 A. This current limit scheme enables ultra-low duty-cycle operation while ensuring robust protection of the regulator.

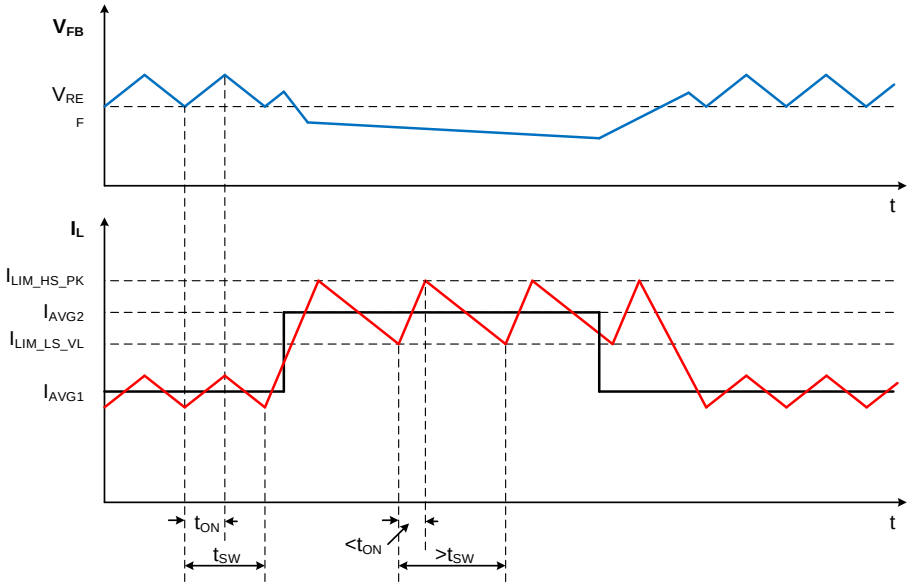


Figure 17. Current Limit Diagram

Power Good (PGOOD)

The power good (PGOOD) pin is an active high, open drain output that indicates if the regulator output voltage is within regulation. High indicates that the voltage at the FB pin (and, hence, the output voltage) is above 95% of the reference voltage. Low indicates that the voltage at the FB pin (and, hence, the output voltage) is below 90% of the reference voltage. PGOOD pin requires a pull-up resistor to a DC supply not greater than 30 V. The typical range of pull-up resistance is 10 kΩ to 100 kΩ. Only SiLM6582 has power good feature.

Working Mode

There are three working modes in the SiLM6582/83: active mode, sleep mode and shutdown mode.

The SiLM6582/83 works in shutdown mode when the voltage on the EN/UVLO pin is below 1.1 V. Both the internal linear regulator and the switching regulator are off. The quiescent current in shutdown mode drops to 15μA.

The SiLM6582/83 works in active mode when the voltage on the EN/UVLO pin is above the enable rising threshold (1.5V typical) and input voltage is above its UVLO threshold. In COT active mode, the SiLM6582/83 is in one of three modes depending on the load current:

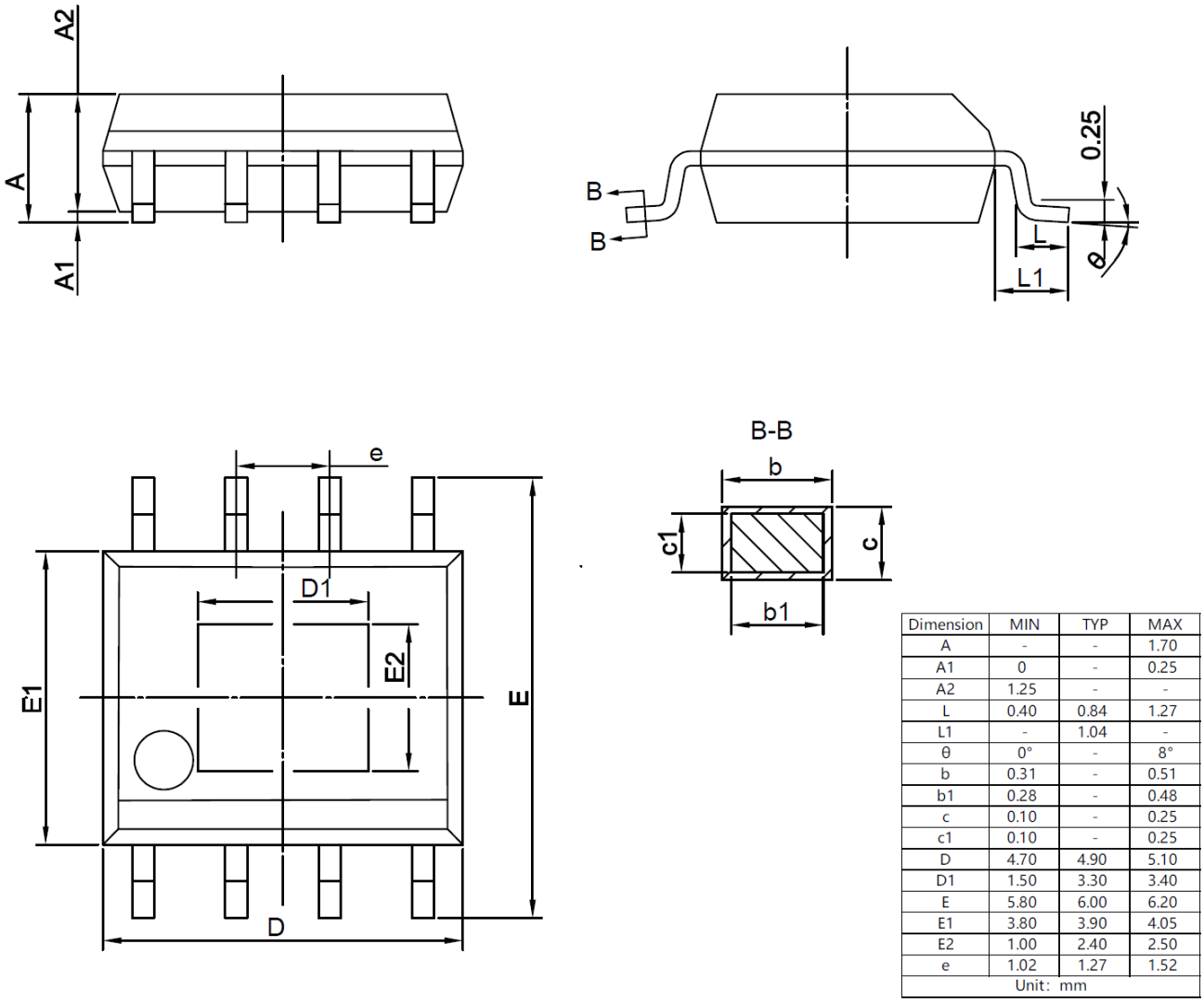
- CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
- Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation
- Current limit CCM with peak and valley current limit protection when an overcurrent condition is applied at the output.

At the light load, as the frequency of operation decreases and V_{FB} remains above 1.2 V with the output capacitor sourcing the load current for greater than 15 μs, the SiLM6582/83 enters sleep mode. The input quiescent current (I_{VIN_SLEEP}) required by the SiLM6582/83 decreases to 20 μA in sleep mode, improving the light-load efficiency of the regulator. In the sleep mode all internal controller circuits are turned off to ensure very low current consumption. Such low I_{VIN_SLEEP} renders the SiLM6582/83 as the best option to extend operating lifetime for off-battery applications. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference and the regulator transitions out of sleep mode into active mode. There is a 9 μs wake-up delay from sleep to active states.

Thermal Protection

In the event that the SiLM6582/83 junction temperature exceeds 175°C, the thermal shutdown circuit turns off the regulator. A 15°C hysteresis is included so that the SiLM6582/83 does not recover from thermal shutdown until the on-chip temperature drops below 160°C. Upon recovery, soft start is initiated prior to normal operation.

PACKAGE CASE OUTLINES



Dimension	MIN	TYP	MAX
A	-	-	1.70
A1	0	-	0.25
A2	1.25	-	-
L	0.40	0.84	1.27
L1	-	1.04	-
θ	0°	-	8°
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.10	-	0.25
c1	0.10	-	0.25
D	4.70	4.90	5.10
D1	1.50	3.30	3.40
E	5.80	6.00	6.20
E1	3.80	3.90	4.05
E2	1.00	2.40	2.50
e	1.02	1.27	1.52
Unit: mm			

Figure 18. SOP8-EP Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Datasheet Rev 1.0: 2024-04-01	
Whole document	Initial release