5.0kV$_{RMS}$ Opto-Compatible Single Channel Isolated Gate Driver

GENERAL DESCRIPTION

The SiLM5347AT isolated driver is an opto-compatible, single channel, isolated MOSFET/IGBT gate driver with 20V UVLO voltage. The peak source current is 4A and sink current is 6A. Key features and characteristics bring significant performance and reliability upgrades over standard opto-coupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, and small pulse width distortion.

The input stage is an emulated diode which means long term reliability and excellent aging characteristics compared to traditional LEDs. It is offered in a SOP6W-T package with ≥8.0mm creepage and clearance. A mold compound from material group II which has a comparative tracking index (CTI) >400V. High performance and reliability of the SiLM5347AT makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

FEATURES

- 4.0A peak source output current
- 6.0A peak sink output current
- 110ns (Max.) propagation delay
- 25ns (Max.) part-to-part delay matching
- 40ns (Max.) pulse width distortion
- 150kV/us (Min.) common mode transient immunity (CMTI)
- Gate drive supply voltage up to 40V
- 30V reverse polarity voltage handling capability on input stage
- Pin to pin compatible to opto-coupler isolated gate drivers
- SOP6W-T package with ≥8.0mm creepage and clearance
- Junction temperature, T_J: –40°C to +150°C
- Safety certifications
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10

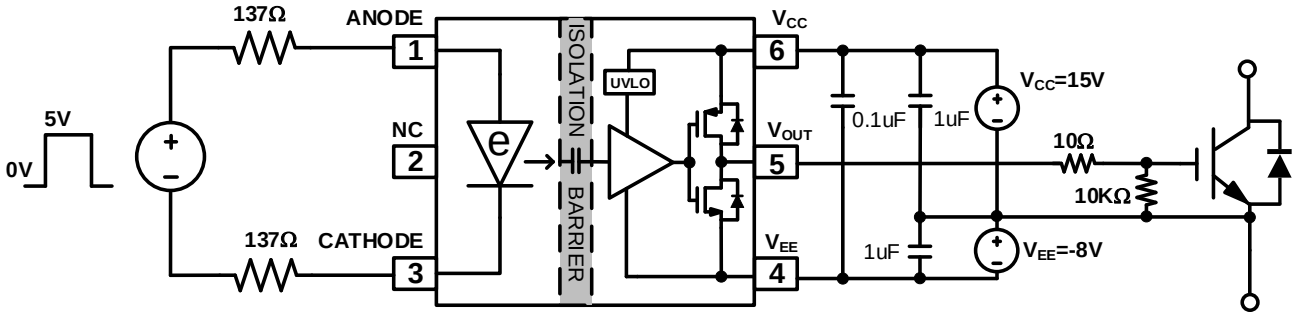


Figure 1. SiLM5347AT Typical Application

Table of Contents

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP6W-T	

PIN DESCRIPTION

No.	Pin	Description
1	ANODE	Anode
2	NC	No Connection
3	CATHODE	Cathode
4	V_{EE}	Negative Power Supply Rail
5	V_{OUT}	Gate Drive Output
6	V_{CC}	Positive Power Supply Rail

FUNCTIONAL BLOCK DIAGRAM

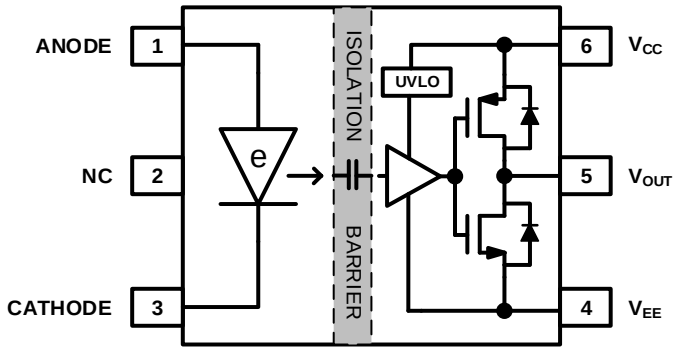


Figure 2. SiLM5347AT Functional Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM5347ATCR-DG	SOP6W-T, Pb-Free	1000/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
$I_{F(AVG)}$	Average Input Current		25	mA
V_R	Reverse Input Voltage		30	V
V_{CC} -V_{EE}	Output supply voltage		45	V
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

RECOMMENDED OPERTION CONDITIONS

Symbol	Definition	Min	Max	Unit
V_{CC} -V_{EE}	Output Supply Voltage	21.5	40	V
I_F(ON)	Input Diode Forward Current (Diode “ON”)	7	16	mA
V_F(OFF)	Anode Voltage - Cathode Voltage (Diode “OFF”)	-30	0.9	V
T_J	Junction temperature	-40	150	°C
T_A	Ambient temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Unit
V_{ESD}	HBM	±4000	V
	CDM	±2000	

THERMAL INFORMATION

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	125	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	66	°C/W
Ψ_{JT}	Junction to top characterization parameter	30	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		0.8		pF
C_{IN}	Input Capacitance		30		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	⩾8	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	⩾8	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>400	V
	Material Group		II	
	Overvoltage category	Rated mains voltages ≤150Vrms	IV	
		Rated mains voltages ≤300Vrms	IV	
		Rated mains voltages ≤600Vrms	III	
		Rated mains voltages ≤1000Vrms	II	
DIN V VDE 0884-11(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577(1)				
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5000	V_{RMS}

1.Certification pending

SAFETY RELATED CERTIFICATIONS

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced Insulation V_{IORM} = 1414 V_{PK} V_{IOTM} = 7000 V_{PK} V_{IOSM} = 6250 V_{PK}	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate, 400 V_{RMS} maximum working voltage
Pending	Pending	Pending

SAFETY LIMITING VALUES

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=125°C/W, V_{CC}-V_{EE} = 30V, T_J =150°C, T_A =25°C	25	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=125°C/W, T_J =150°C, T_A =25°C	750	mW
T_S	Maximum safety temperature		150	°C

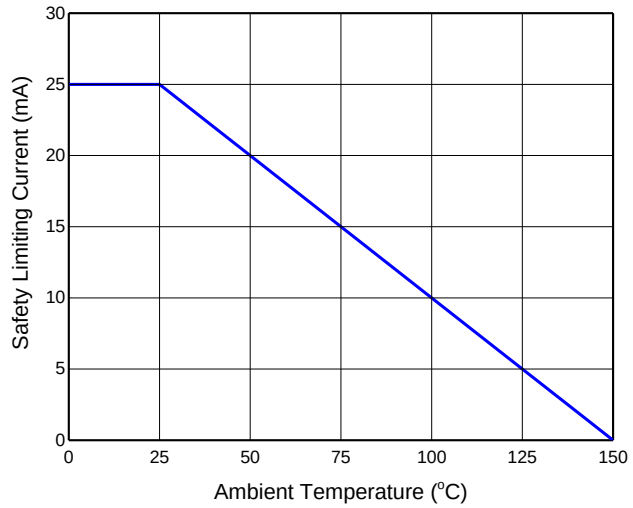


Figure 3. Thermal Derating Curve for Limiting Current per VDE

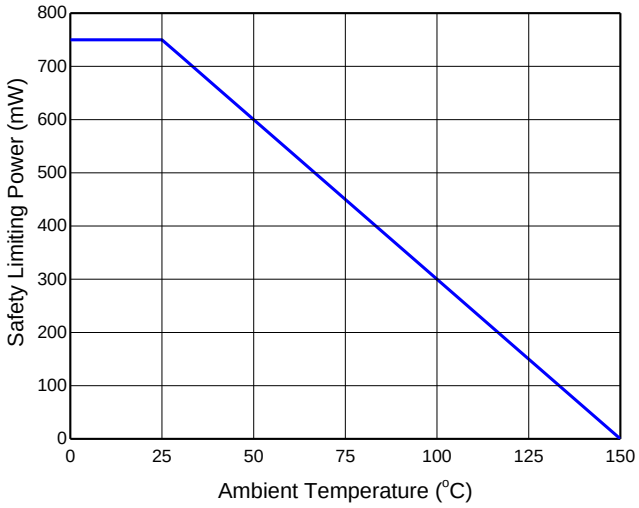


Figure 4. Thermal Derating Curve for Limiting Power per VDE

ELECTRIAL CHARACTERISTICS (DC)

V_{CC}-V_{EE} = 25V, V_{EE} = GND and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
INPUT						
I_{FLH}	Input Forward Threshold Current Low to High		1.6	2.1	3	mA
V_F	Input Forward Voltage	I_F=10mA	2.1	2.25	2.5	V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	I_F=10mA		0.5		mV/°C
V_R	Input Reverse Breakdown Voltage	I_R=10uA	30			V
OUTPUT						
I_{OH}	High Level Peak Output Current	V_{CC}=25V,I_F=10mA, C_{VDD}=10uF, C_{LOAD}=220nF		4.0		A
I_{OL}	Low Level Peak Output Current	V_{CC}=25V, V_F=0V, C_{VDD}=10uF, C_{LOAD}=220nF		6.0		A
V_{OH}	High Level Output Voltage	I_F=10mA, I_O=-20mA “With respect to Vcc”		26		mV
V_{OL}	Low Level Output Voltage	V_F=0V, I_O=20mA		13		mV
UNDER VOLTAGE LOCKOUT						
$UVLO_R$	Under Voltage Lockout V_{CC} rising	I_F=10mA	18.5	20	21.5	V
$UVLO_F$	Under Voltage Lockout V_{CC} falling	I_F=10mA	17	18.5	20	V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			1.5		V

SWITCHING CHARACTERISTICS (AC)

V_{CC}-V_{EE} = 25V, V_{EE} = GND and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation delay, Low to High	C_{LOAD} =1nF, f_{sw}=20kHz, (50% Duty Cycle), V_{CC}=25V		75	110	ns
t_{PHL}	Propagation delay, High to Low			75	110	ns
t_r	Turn on rise time				25	ns
t_f	Turn off fall time				15	ns
t_{PWD}	Pulse Width Distortion				40	ns
t_{PDD}	Propagation Delay Difference Between Any Two Parts				25	ns
t_{UVLO_REC}	UVLO Recovery Delay	V_{CC} Rising from 0V to 25V		22	30	us
$CMTI_H$	Output High Level Common Mode Transient Immunity	I_F=10mA, V_{CM}=1000V, V_{CC}=25V, T_A=25°C	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_F=0V, V_{CM}=1000V, V_{CC}=25V, T_A=25°C	150	200		kV/us

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 5 shows the propagation delay from the input forward current I_F,to V_{OUT}. This figure also shows the circuit used to measure the rise (t_r)and fall(t_f) times and the propagation delays t_{PDLH} and t_{PDHL}.

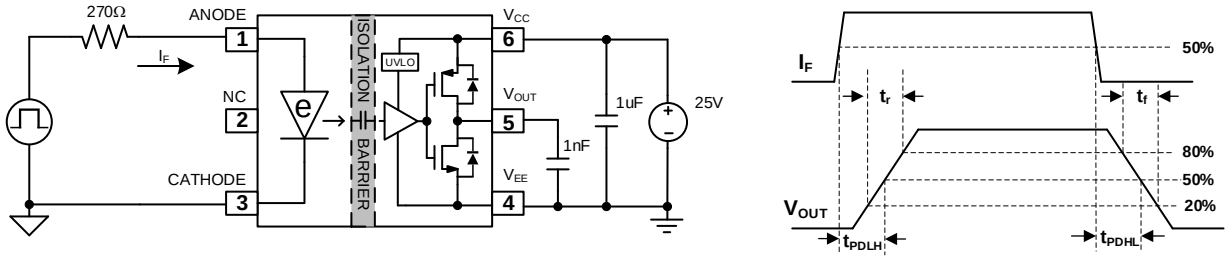


Figure 5. Propagation Delay, Rise Time and Fall Time

IOH and IOL Testing

Figure 6 shows the circuit used to measure the output drive current I_{OL} and I_{OH}. A load capacitance of 220nF is used at the output. The peak dv/dt of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

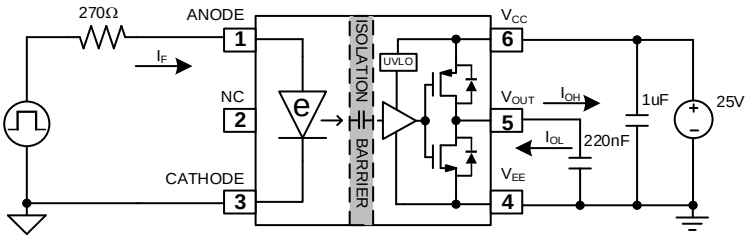


Figure 6. I_{OH} and I_{OL}

CMTI Testing

Figure 7 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V. The test is performed with I_F=10mA (V_{OUT}= High) and V_F=0V (V_{OUT}= Low).

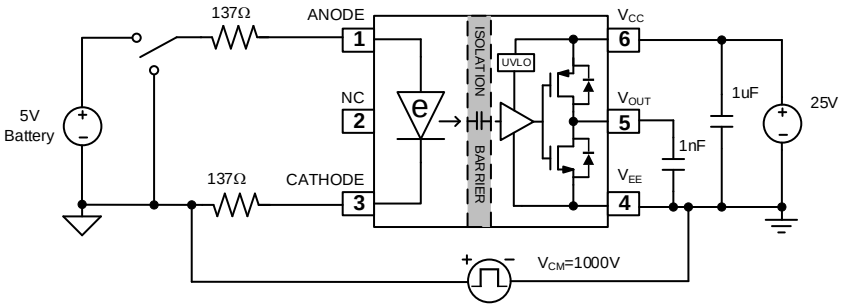


Figure 7. CMTI Test Circuit

FEATURE DESCRIPTION

SiLM5347AT is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs and MOSFETs. It has 4.0A peak output current capability with maxim output driver supply voltage of 40V. The inputs and the outputs are galvanically isolated. SiLM5347AT is offered in SOP6W-T package with >8.5mm creepage and clearance. The reinforced isolation rating is $5kV_{RMS}$ for 60 seconds. It is pin-to-pin compatible with standard opto-coupler isolated gate drivers. While standard opto-coupler isolated gate drivers use an LED as the input stage, SiLM5347AT uses an emulated diode as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV SiO2 capacitors in full differential configuration that not only provides reinforced isolation but also offers great performance of common mode transient immunity >150kV/us. The e-diode input stage along with capacitive isolation technology gives SiLM5347AT several performance advantages over standard opto-coupler isolated gate drivers.

- Since the emulated diode does not use light emission for its operation, the reliability and aging characteristics of SiLM5347AT are naturally superior to those of standard opto-coupler isolated gate drivers.
- Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto-coupler isolated gate drivers
- The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature
- Higher common mode transient immunity than opto-coupler isolated gate drivers
- Smaller propagation delay than opto-coupler isolated gate drivers
- Due to superior process controls achievable in capacitive isolation compared to opto-coupler isolation, there is less part-to-part skew in the propagation delay, making the system design simpler and more robust
- Smaller pulse width distortion than opto-coupler isolated gate drivers

Input Stage

The input stage of SiLM5347AT is an emulated diode. When the emulated diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current, I_F, flows into the e-diode. The forward voltage drop across the e-diode is 2.25V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7mA to 16mA. When I_F exceeds the input forward threshold current I_{FLH} (2.1mA typ), the V_{OUT} is driver high. If the I_F is lower than I_{FLH}, or the voltage between Anode and Cathode is reverse biased, the V_{OUT} is driven low.

The reverse breakdown voltage of the e-diode is up to 30V. The large reverse breakdown voltage of the e-diode enables SiLM5347AT to be operated in interlock architecture as shown in Figure 8. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown in Figure 8 and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

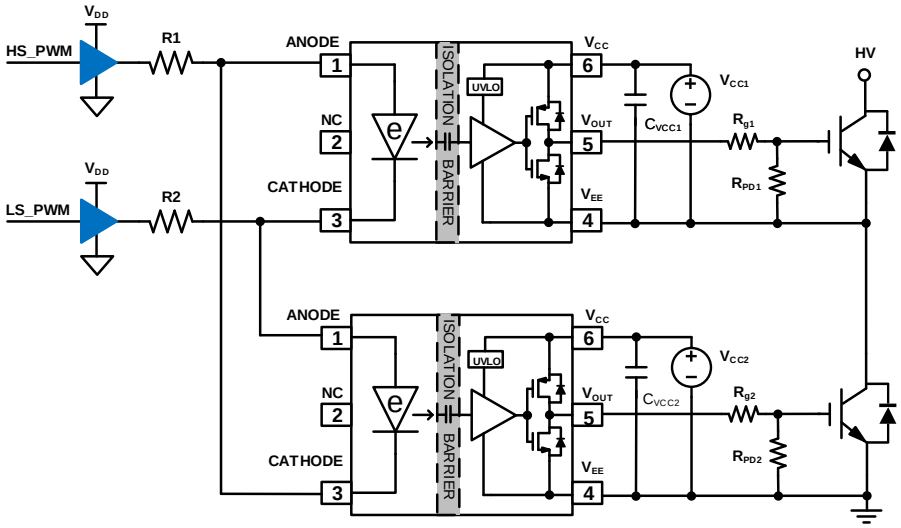


Figure 8. Interlock Architecture

Under Voltage Lockout (UVLO)

The SiLM5347AT integrates the UVLO protection on the V_{CC} to prevent an under driven condition on IGBTs and MOSFETs. When V_{CC} is lower than $UVLO_R$ during start up or lower than $UVLO_F$ after start up, the UVLO feature holds the V_{OUT} low, regardless of the input forward current. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply. When V_{CC} drops below $UVLO_F$, a recovery delay (t_{UVLO_REC}) occurs on the output when the supply voltage rises above $UVLO_R$ again.

Typical Input Configuration Circuit

The circuit in Figure 9 and Figure 10 show two typical input configuration circuits for SiLM5347AT to driver IGBT.

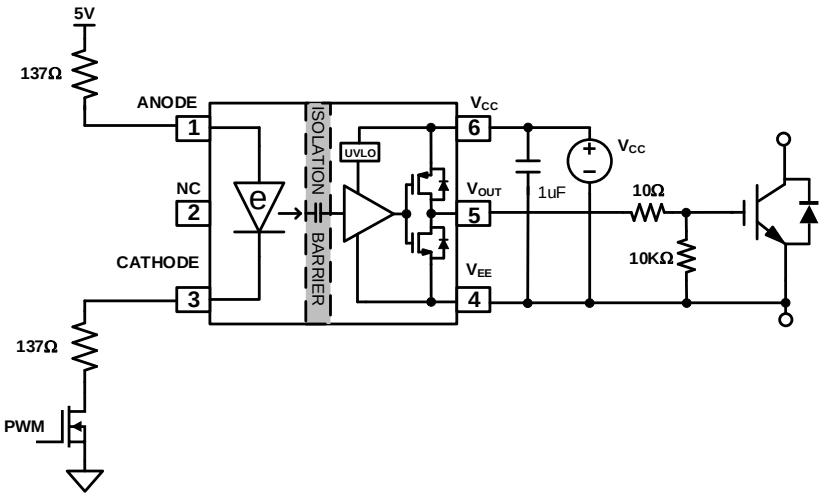


Figure 9. Single MOSFET Circuit as Input Drive of SiLM5347AT to Drive IGBT

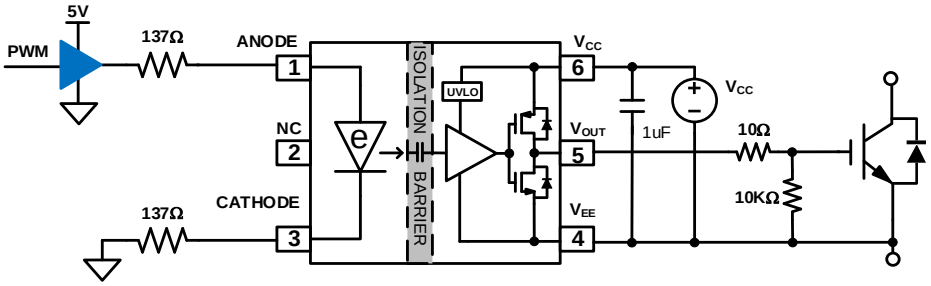


Figure 10. Buffer Circuit as Input Drive of SiLM5347AT to Drive IGBT

Layout

In order to achieve optimum performance for the SiLM5347AT, some suggestions on PCB layout.

Component placement:

- Low ESR and low ESL capacitors must be connected close to the device between the V_{CC} and V_{EE} pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the VEE pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

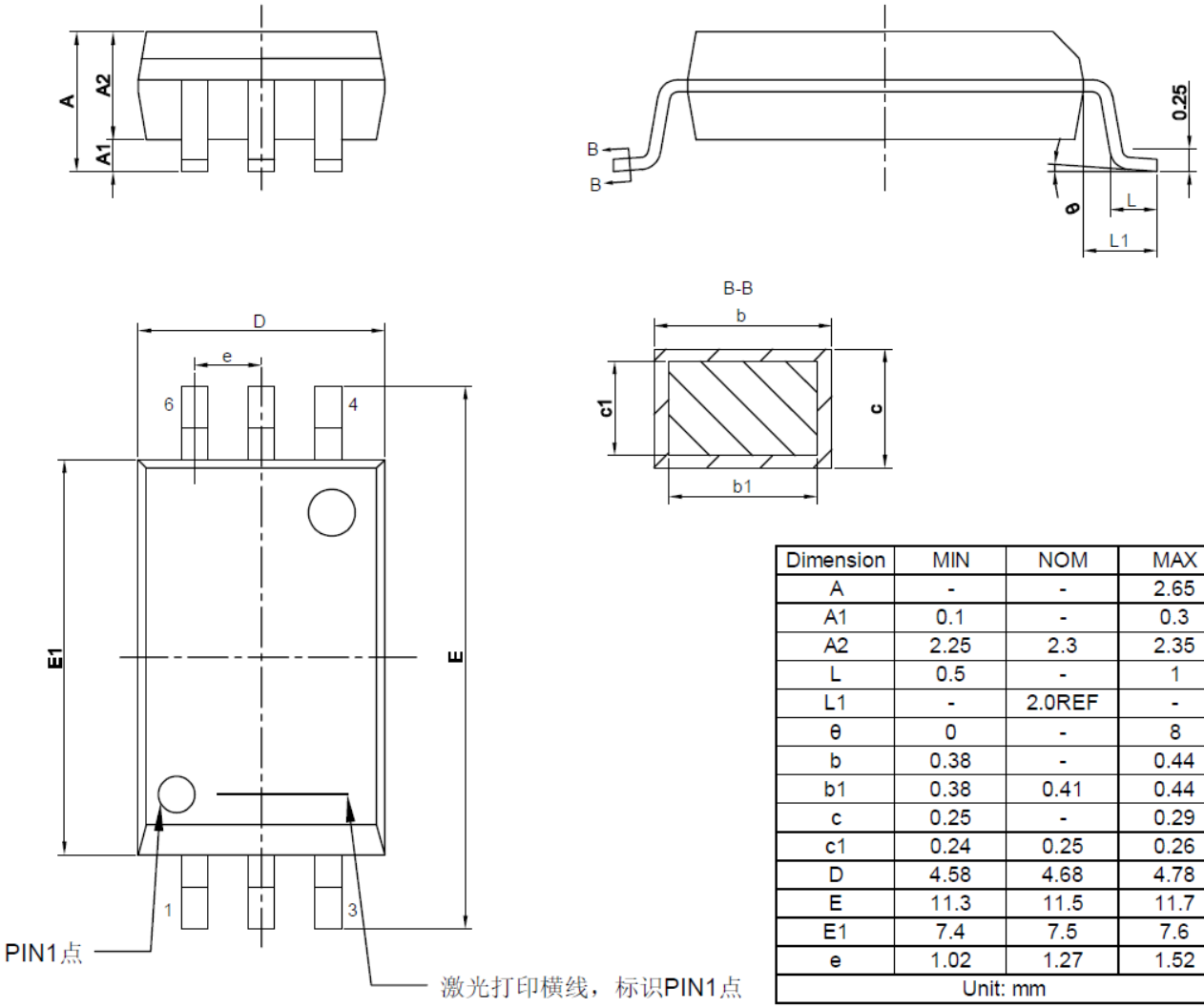
Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

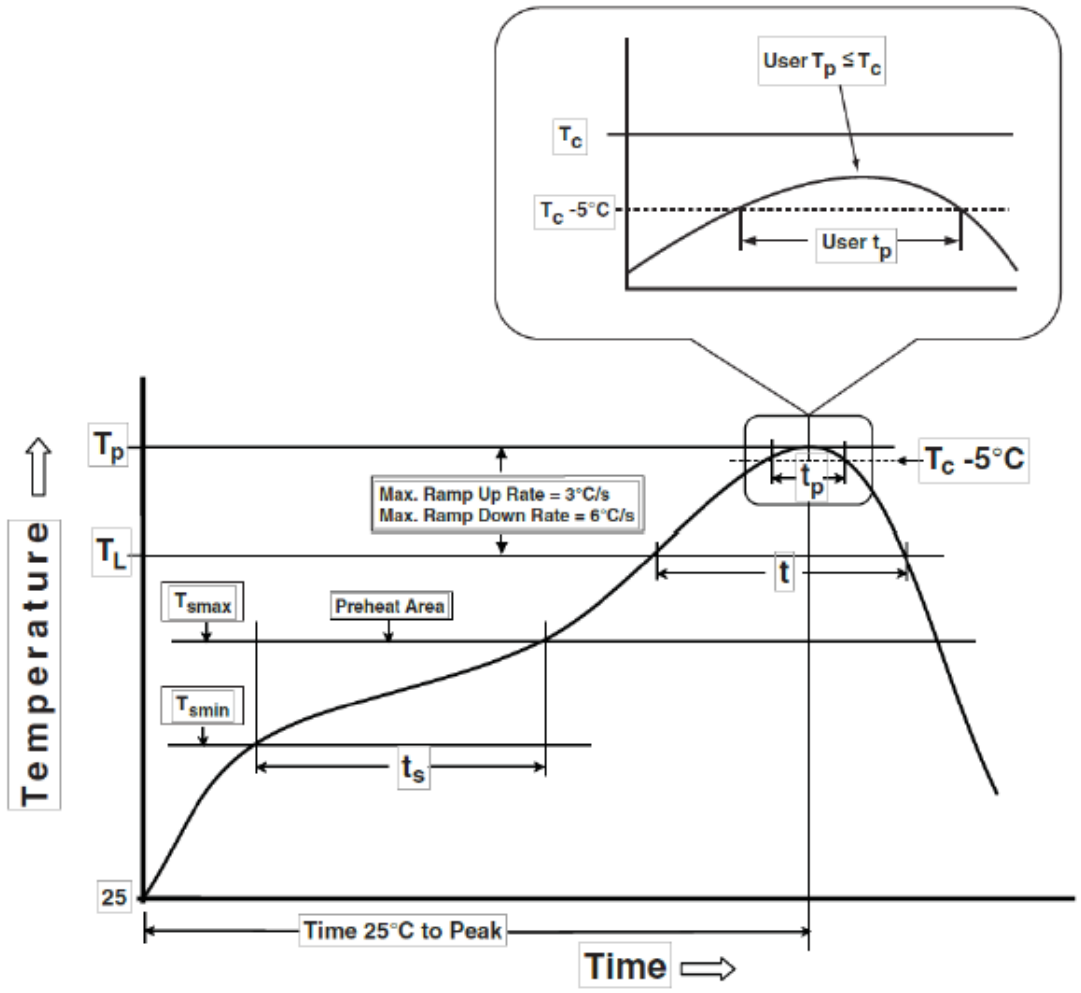
PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.25	2.3	2.35
L	0.5	-	1
L1	-	2.0REF	-
θ	0	-	8
b	0.38	-	0.44
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	4.58	4.68	4.78
E	11.3	11.5	11.7
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit: mm			

Figure 11. SOP6W-T Package Outline Dimensions

REFLOW PROFILE GUIDANCE



Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150 °C 200 °C 60-120 seconds
Ramp-up rate (TL to Tp)	3 °C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217 °C 60-150 seconds
Peak package body temperature (Tp)	TC ： 260 °C （for user：The peak temperature must not exceed 260 °C.）
Time (tp)* within 5 °C of the specified classification temperature (Tc)	30 seconds （for user：The time above 255 °C must not exceed 30 seconds.）
Ramp-down rate (Tp to TL)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-11-29	
Whole document	Initial datasheet release