600V 3-Phase Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/-** 200 mA / 350 mA
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 480 ns / 370 ns
- **Deadtime (typ.)** 290 ns

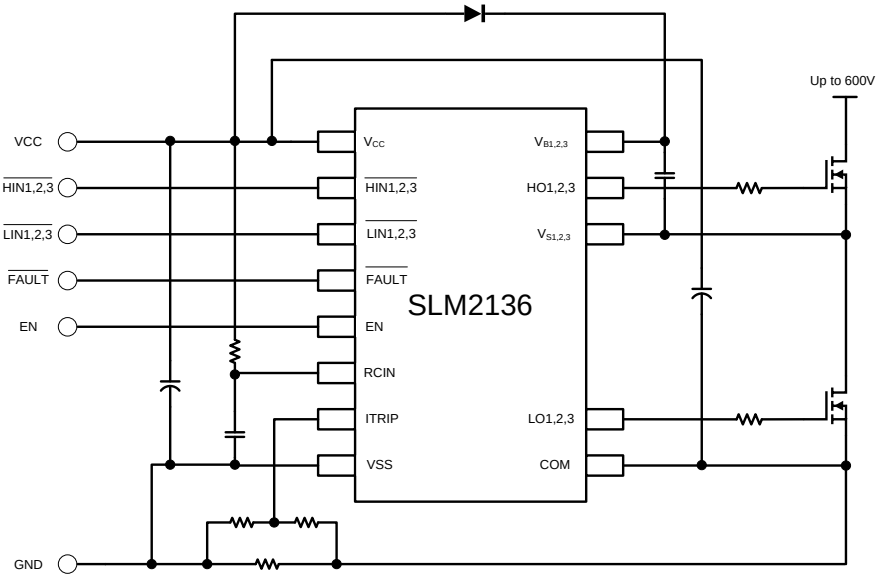
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Low/high side output out of phase with inputs
- 3.3 V, 5 V, and 15 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Externally programmable delay for automatic fault clear
- SOP28W package

GENERAL DESCRIPTION

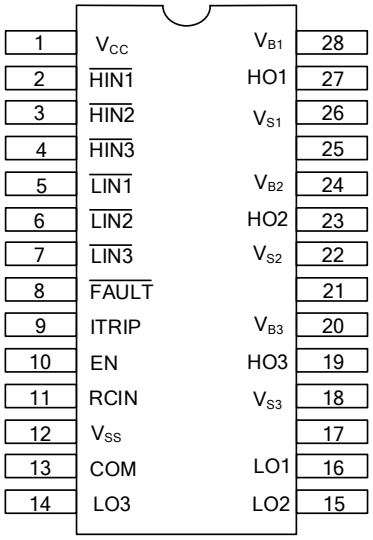
The SLM2136 is a high voltage, high speed power MOSFET and IGBT drivers for 3-phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

TYPICAL APPLICATION CIRCUIT



Refer to Pin Configuration for correct configuration. This diagram shows electrical connections only.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP28W	

PIN DESCRIPTION

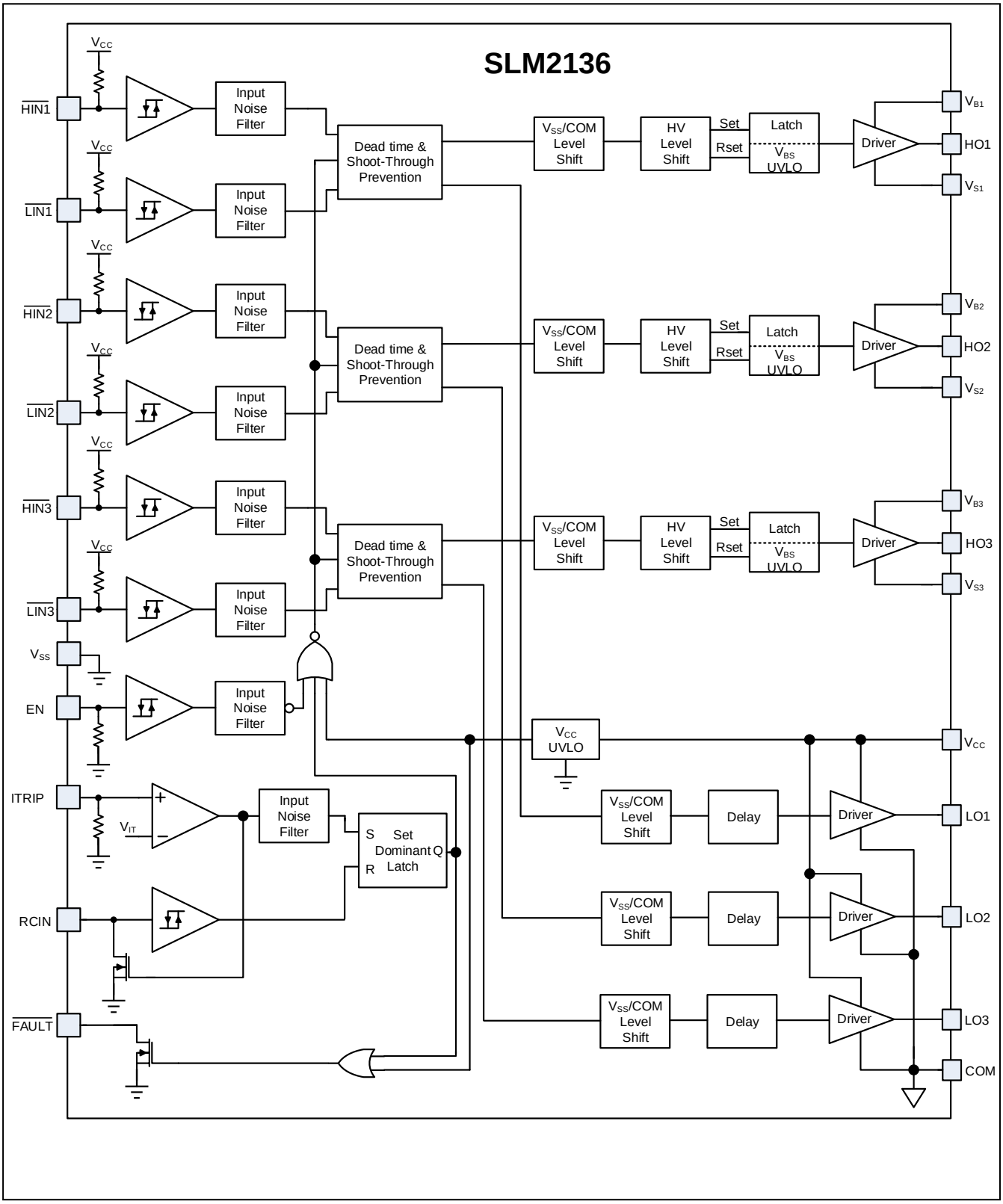
No.	Pin	Description
1	V_{CC}	Low-side and logic fixed supply.
2, 3, 4	$\overline{HIN1, 2, 3}$	Logic input for high-side gate driver output (HO), out of phase.
5, 6, 7	$\overline{LIN1, 2, 3}$	Logic input for low-side gate driver output (LO), out of phase.
8	$\overline{FAULT}$	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output.
9	ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
10	EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. No effect on FAULT and not latched.
11	RCIN	External RC network input used to define FAULT CLEAR delay, TFLTCLR, approximately equal to R*C. When RCIN>8 V, the FAULT pin goes back into open-drain high-impedance.
12	V_{SS}	Logic ground.
13	COM	Low-side gate drivers return.
14, 15, 16	LO1, 2, 3	Low-side gate driver outputs.
18, 22, 26	$V_{S1, 2, 3}$	High-side floating supply return.
19, 23, 27	HO1, 2, 3	High-side gate driver outputs.
20, 24, 28	$V_{B1, 2, 3}$	High-side floating supply.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2136CF-DG	SOP28W, Pb-Free	1000/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
V_{HO}	High-side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	-5	+5	
V_{IN}	Logic input voltage (LIN, HIN, ITRIP, EN, RCIN)	V_{SS} - 0.3	Lower of (V_{SS} + 25) or (V_{CC} + 0.3)	
$V_{LO1,2,3}$	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{RCIN}	RCIN input voltage	V_{SS} - 0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage	V_{SS} - 0.3	Lower of (V_{SS} + 25) or (V_{CC} + 0.3)	
dV_S/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant$ +25°C	---	1.6	W
θ_{JA}	Thermal resistance, junction to ambient	---	75	°C/W
T_J	Junction temperature	---	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High-side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High-side floating supply offset voltage		600	
$V_{HO1,2,3}$	High-side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low-side output voltage	0	V_{CC}	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{SS}	Logic ground	-5	5	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} + 20V	
V_{IN}	Logic input voltage $\overline{\text{LIN1, 2, 3}}$, $\overline{\text{HIN1, 2, 3}}$	V_{SS}	V_{SS} + 20V	
T_A	Ambient temperature	- 40	125	°C

Note: Logic operational for V_S of (COM – 5 V) to (COM + 600V). Logic state held for V_S of (COM-5V) to (COM - V_{BS}).

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, $V_{S1,2,3}$ = V_{SS} = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	300	480	600	ns
t_{off}	Turn-off propagation delay	V_S = 600 V	250	370	550	
t_r	Turn-on rise time		---	125	190	
t_f	Turn-off fall time		---	50	75	
t_{EN}	Enable low to output shutdown propagation delay	V_{IN}, V_{EN} = 0 V or 5 V	300	450	600	
t_{ITRIP}	ITRIP to output shutdown propagation delay	V_{ITRIP} = 5 V	450	650	850	
t_{bl}	ITRIP blanking time	V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V	100	150	---	
t_{FLT}	ITRIP to $\overline{FAULT}$ propagation delay	V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V	400	630	800	
t_{FILIN}	Input filter time (HIN, LIN)	V_{IN} = 0 V & 5 V	200	300	---	
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1nF	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V	1.3	1.8	2	ms
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	V_{IN} = 0 V & 5 V	200	290	450	ns
MT	Matching delay, HS & LS turn-on/off	External dead time > 400 ns	---	30	90	
PM	Output pulse width matching (pwin - pwout) (Figure 2)		---	40	75	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all 6 channels ($\overline{LIN1, 2, 3}$ and $\overline{HIN1, 2, 3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “0” input voltage ($\overline{LIN1, 2, 3}$ and $\overline{HIN1, 2, 3}$)	V_{CC} = 10 V to 20V	---	---	2.5	V
V_{IL}	Logic “1” input voltage ($\overline{LIN1, 2, 3}$ and $\overline{HIN1, 2, 3}$)		0.8	---	---	
$V_{EN, TH+}$	Enable positive going threshold		---	---	1.7	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{EN, TH-}$	Enable negative going threshold		1.0	---	---	
$V_{IT, TH+}$	ITRIP positive going threshold		0.39	0.47	0.55	
$V_{IT, HYS}$	ITRIP input hysteresis		---	0.1	---	V
$V_{RCIN, TH+}$	RCIN positive going threshold		---	8	---	
$V_{RCIN, HYS}$	RCIN input hysteresis		---	1	---	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	---	0.5	1.0	
V_{OL}	Low level output voltage, V_O		---	0.3	0.6	
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold		8.0	8.9	9.8	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold		7.4	8.2	9.0	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis		0.3	0.7	---	
V_{IN_CLAMP}	Input clamp voltage (HIN, LIN, ITRIP and EN)	I_{IN} = 100 µA	---	6.8	---	
I_{LK}	Offset supply leakage current	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V	---	60	75	
I_{QCC}	Quiescent V_{CC} supply current		---	1.6	2.3	mA
I_{IN+}	Logic “1” input bias current	$\overline{HIN1, 2, 3}$ = 0 V, $\overline{LIN1, 2, 3}$ = 0 V	---	250	300	µA
I_{IN-}	Logic “0” input bias current	$\overline{HIN1, 2, 3}$ = 5 V, $\overline{LIN1, 2, 3}$ = 5 V	---	150	200	
I_{ITRIP+}	“High” ITRIP input bias current	V_{ITRIP} = 5 V	---	36	100	
I_{ITRIP-}	“Low” ITRIP input bias current	V_{ITRIP} = 0 V	---	0	1	
I_{EN+}	“High” ENABLE input bias current	V_{ENABLE} = 5 V	---	40	100	
I_{EN-}	“Low” ENABLE input bias current	V_{ENABLE} = 0 V	---	0	1	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{RCIN}	RCIN input bias current	V_{RCIN} = 0 V or 15 V	---	0	1	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = V_{IH} PW ⩽ 10 μs	120	200	---	mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = V_{IL} PW ⩽ 10 μs	250	350	---	
R_{on_RCIN}	RCIN low on resistance		---	25	50	Ω
R_{on_FAULT}	$\overline{FAULT}$ low on resistance		---	120	200	

FUNCTIONAL TABLE

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
< UVCC	X	X	X	0 (note 2)	0	0
15 V	< UVBS	0 V	5 V	High imp	LIN1,2,3	0
15 V	15 V	0 V	5 V	High imp	LIN1,2,3 (note 1)	HIN1,2,3 (note 1)
15 V	15 V	> V_{ITRIP}	5 V	0 (note 3)	0	0
15 V	15 V	0 V	0 V	High imp	0	0

Note:

1. A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
2. U_{VCC} is not latched, when V_{CC} > U_{VCC}, FAULT returns to high impedance.
3. When ITRIP < V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V).

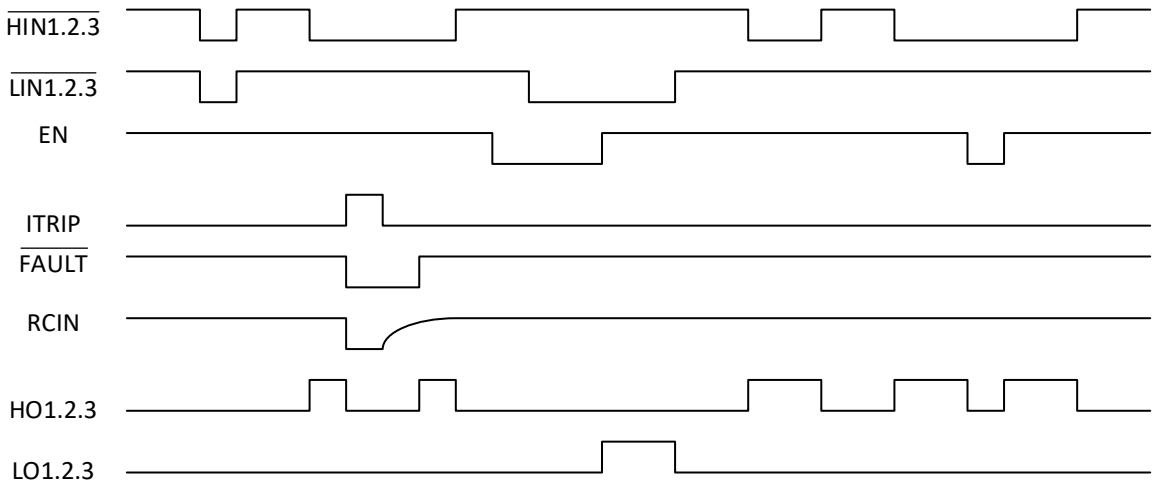


Figure 1. Input/output Timing Diagram

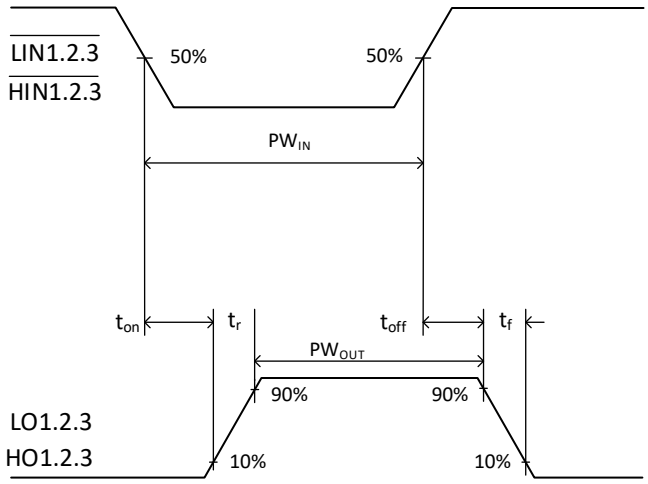


Figure 2. Switching Time Waveforms

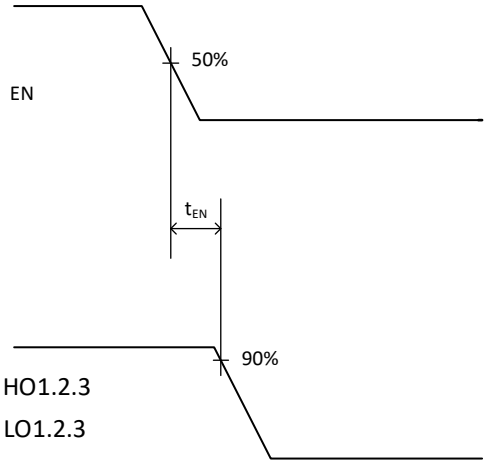


Figure 3. Output Enable Timing Waveform

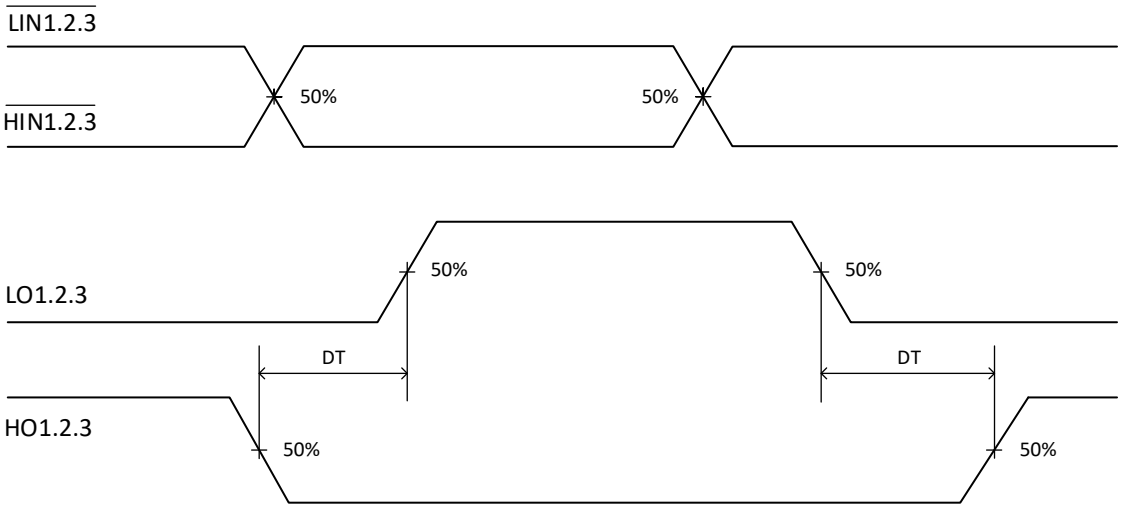


Figure 4. Internal Deadtime Timing Waveforms

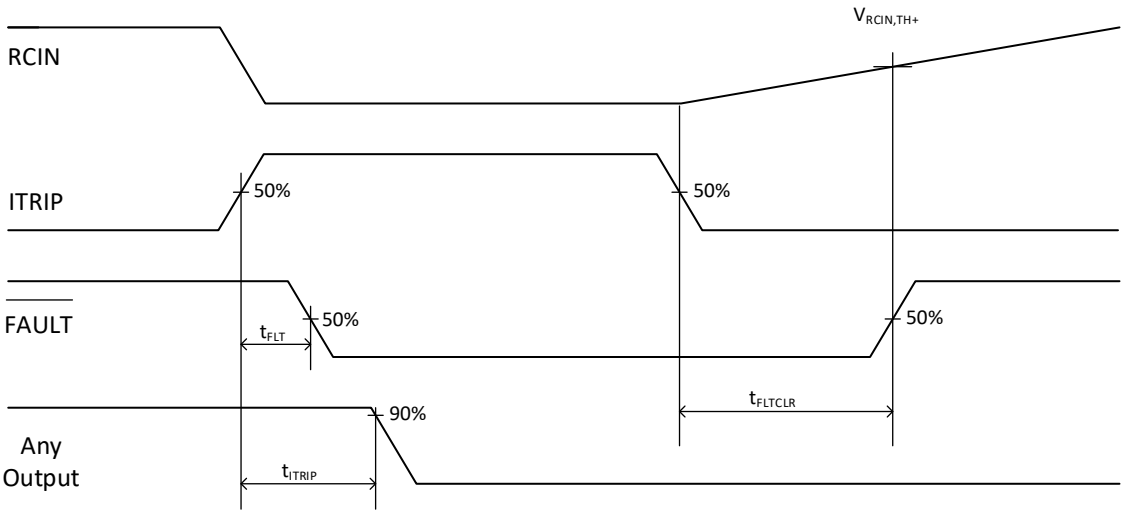


Figure 5. ITRIP/RCIN Timing Waveforms

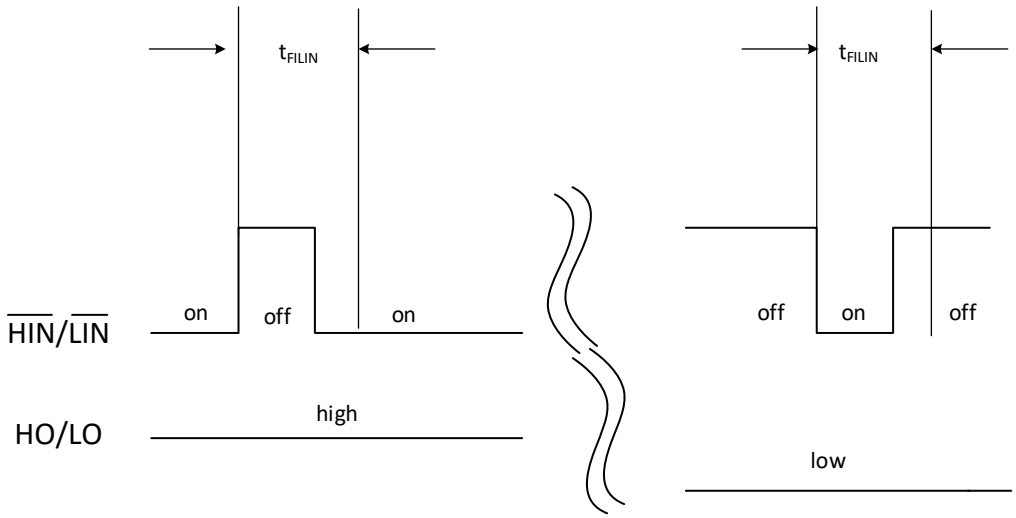
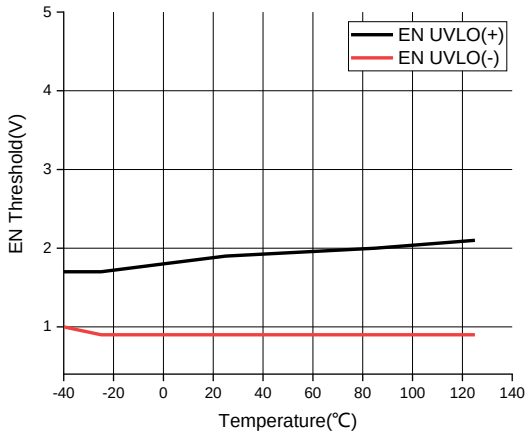
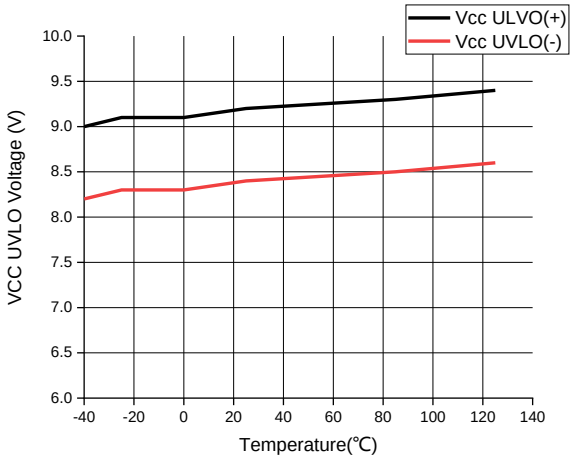


Figure 6. Input Filter Function

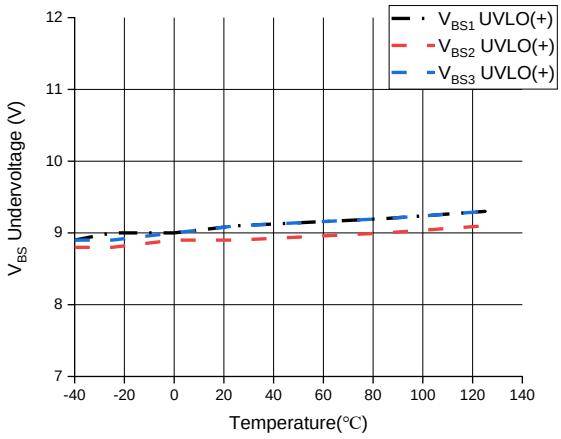
TYPICAL PERFORMANCE CHARACTERISTICS



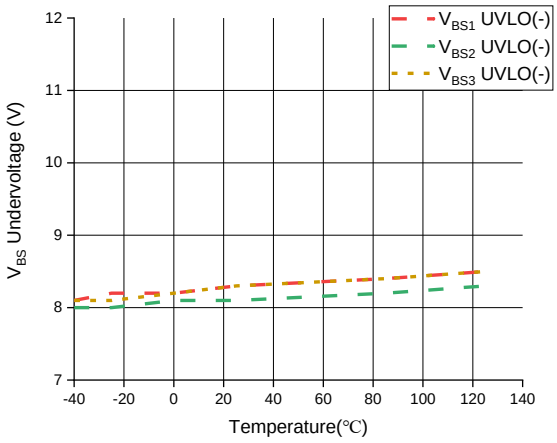
EN Threshold Voltage vs. Temperature



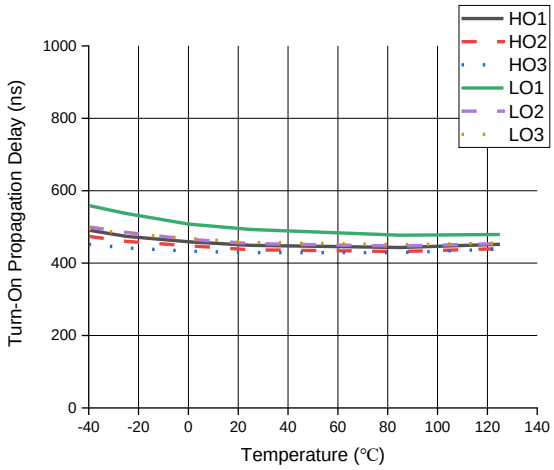
VCC Threshold Voltage vs. Temperature



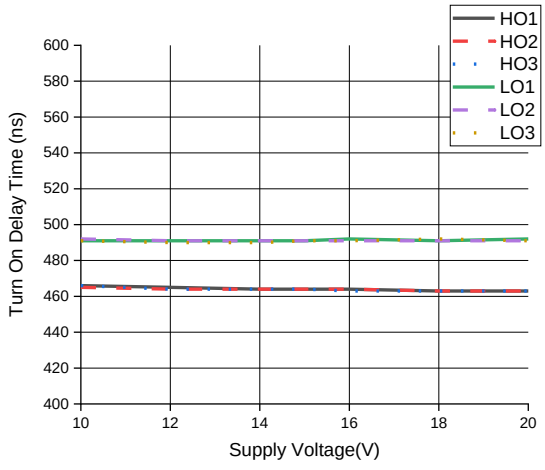
V_{BS} Undervoltage (+)vs. Temperature



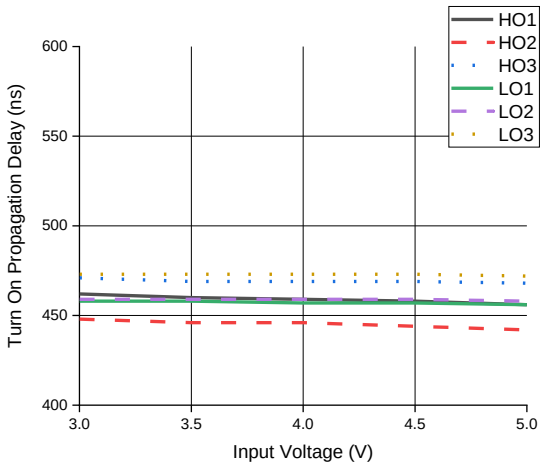
V_{BS} Undervoltage (-) vs. Temperature



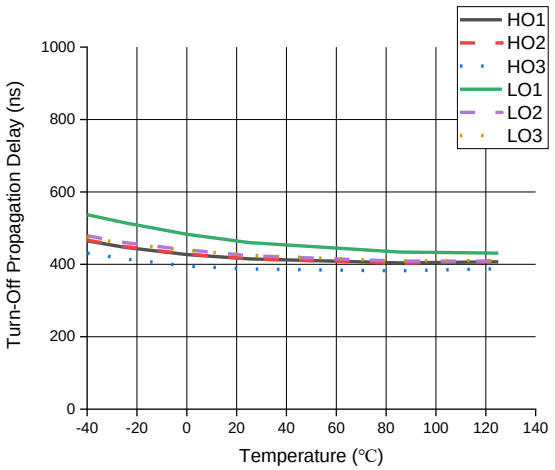
Turn-On Propagation Delay vs. Temperature



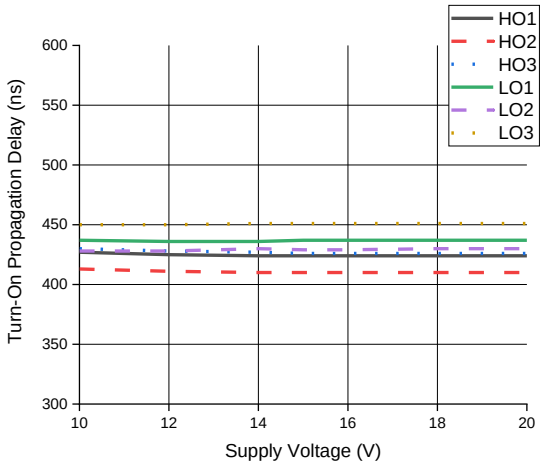
Turn-On Propagation Delay vs. Supply Voltage



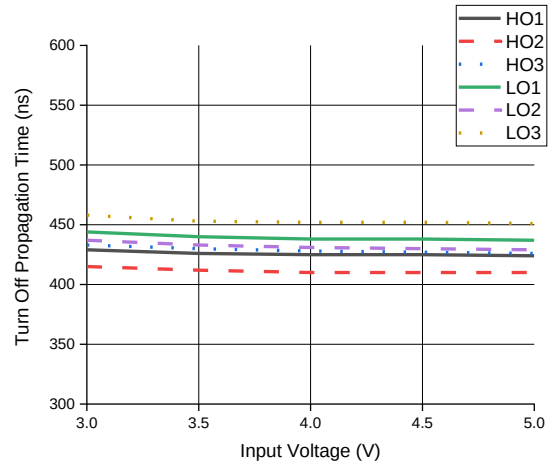
Turn-On Propagation Delay vs. Input Voltage



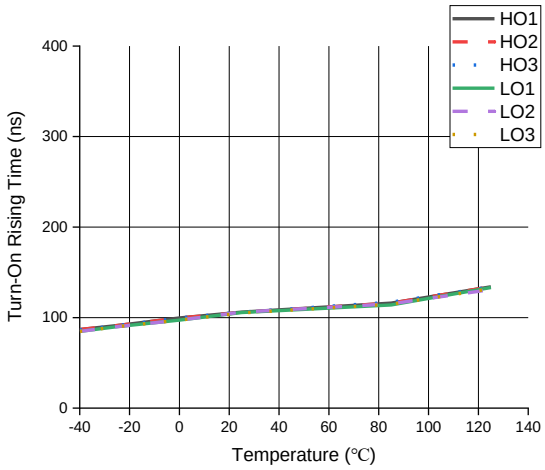
Turn-Off Propagation Delay vs. Temperature



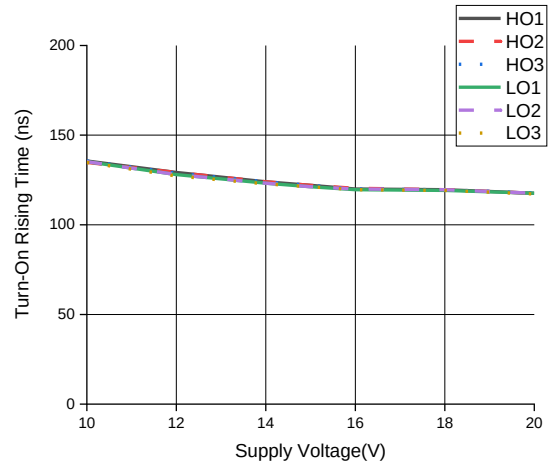
Turn-Off Propagation Delay vs. Supply Voltage



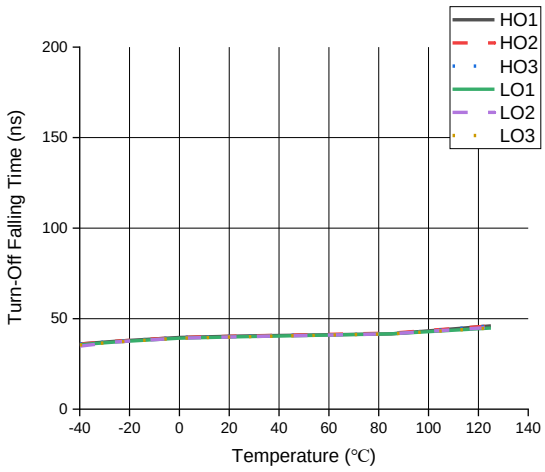
Turn-Off Propagation Delay vs. Input Voltage



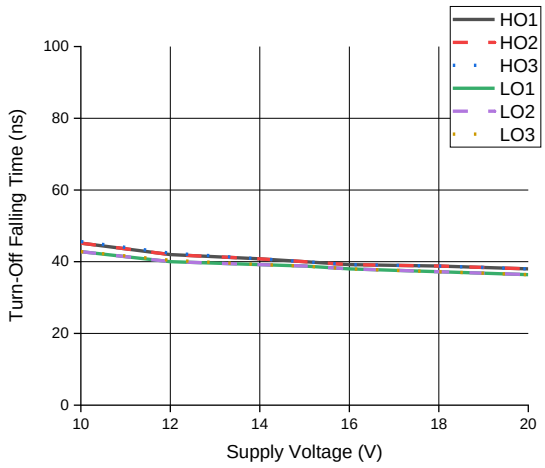
Turn-On Rise Time vs. Temperature



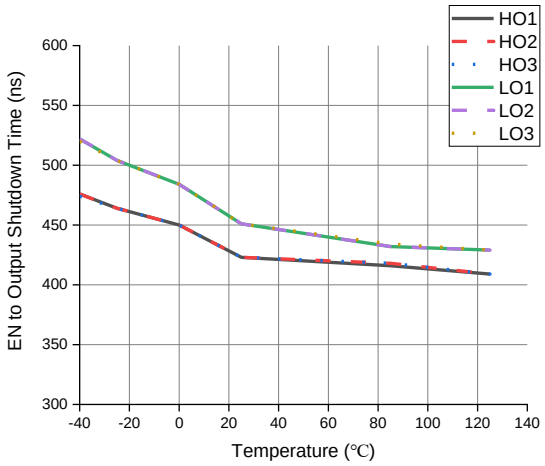
Turn-On Rise Time vs. Supply Voltage



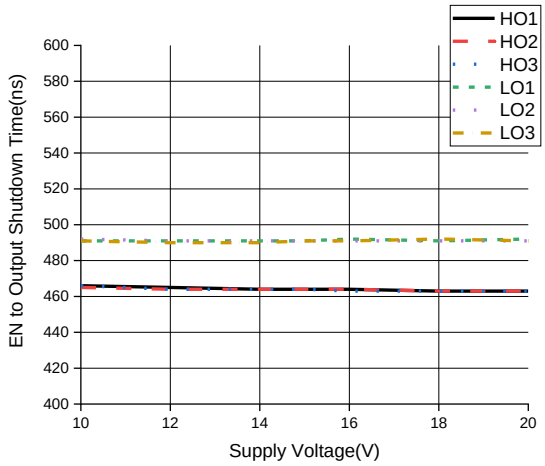
Turn-Off Fall Time vs. Temperature



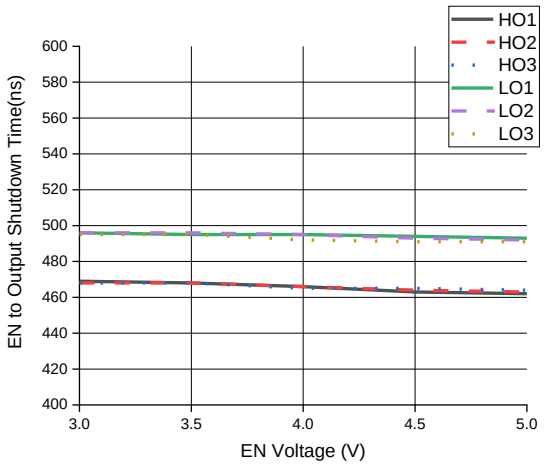
Turn-Off Fall Time vs. Supply Voltage



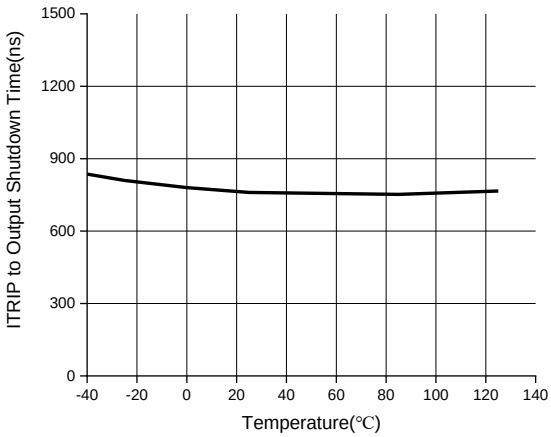
EN to Output Shutdown Time vs. Temperature



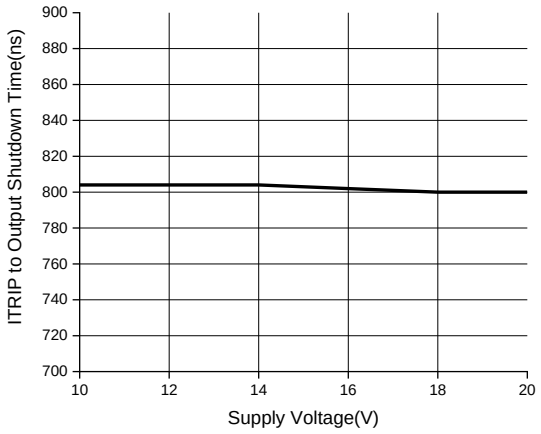
EN to Output Shutdown Time vs. Supply Voltage



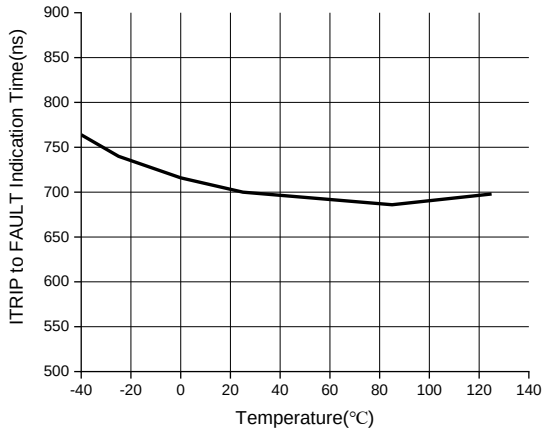
EN To Output Shutdown Time vs. EN Voltage



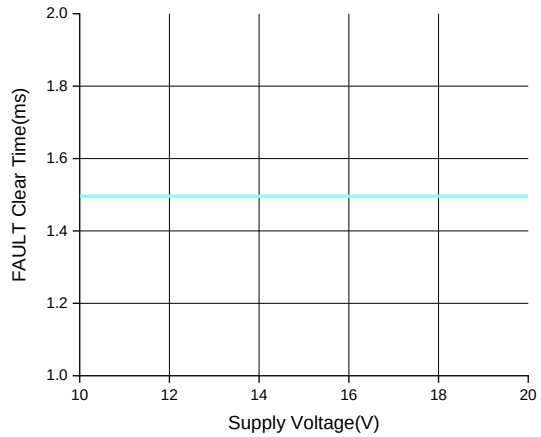
ITRIP To Output Shutdown Time vs. Temperature



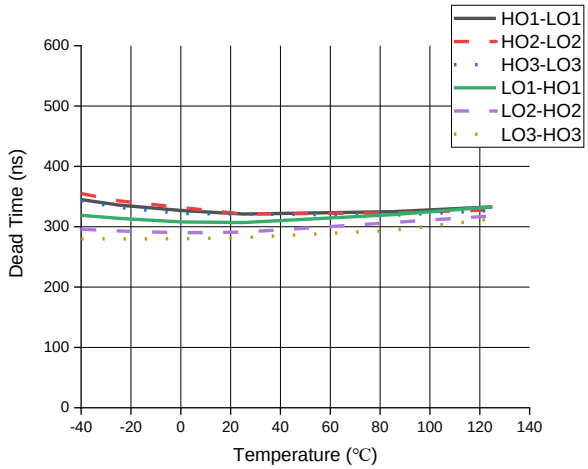
ITRIP To Output Shutdown Time vs. Supply Voltage



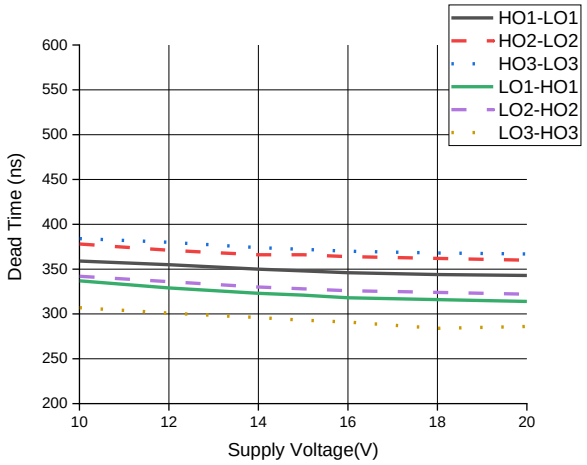
ITRIP To FAULT Indication Time vs. Temperature



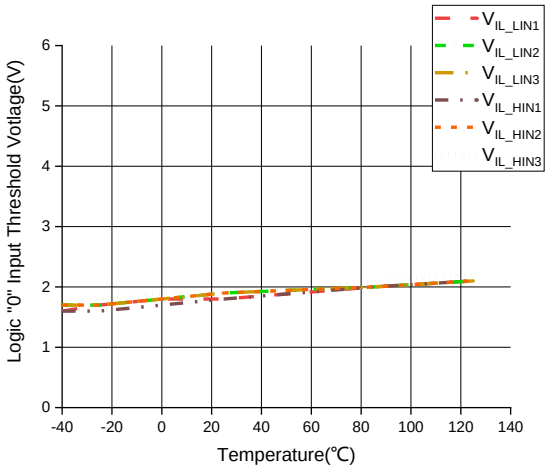
FAULT Clear Time vs. Supply Voltage



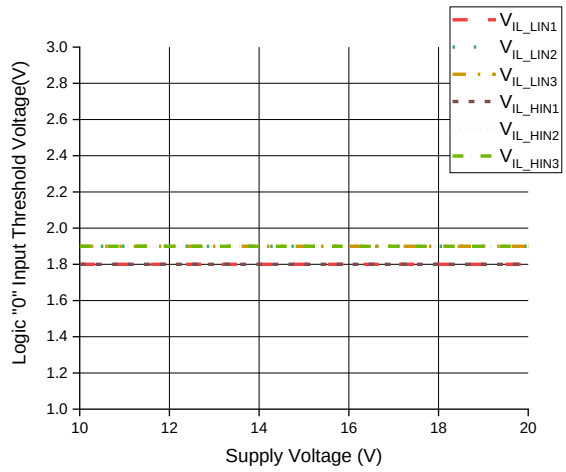
Deadtime vs. Temperature



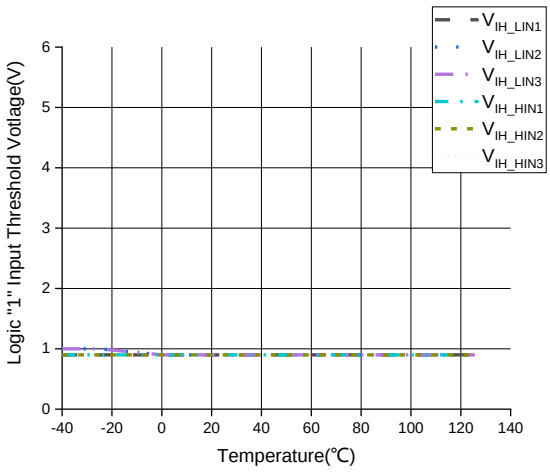
Deadtime vs. Supply voltage



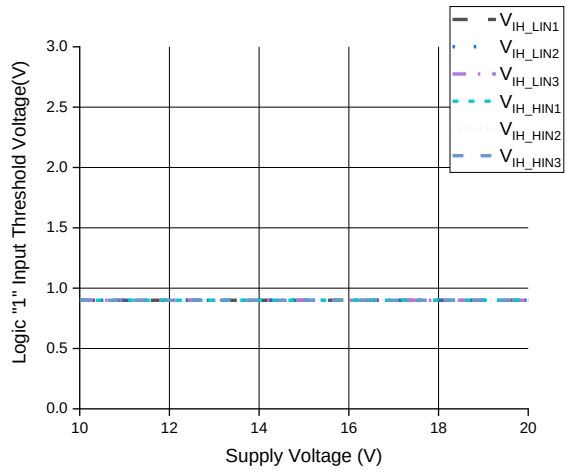
Logic "0" Input Threshold Voltage vs. Temperature



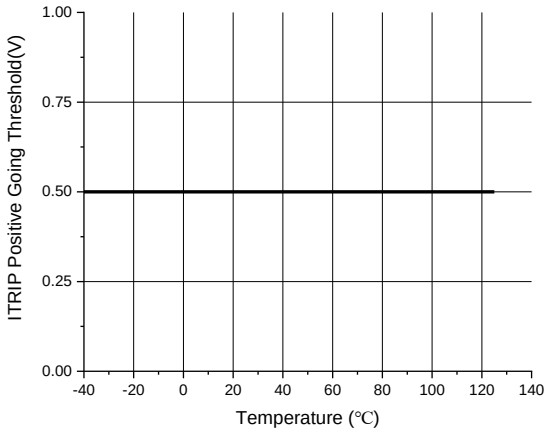
Logic "0" Input Threshold vs. Supply Voltage



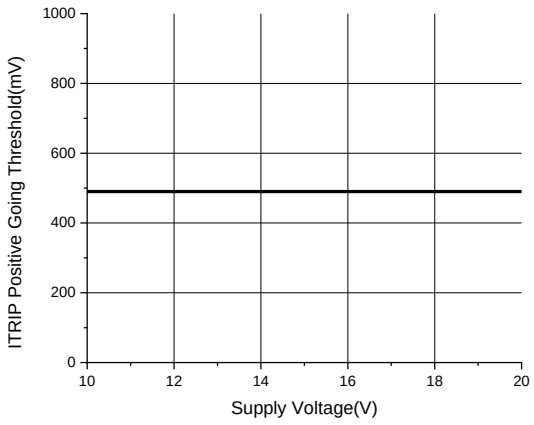
Logic "1" Input Threshold Voltage vs. Temperature



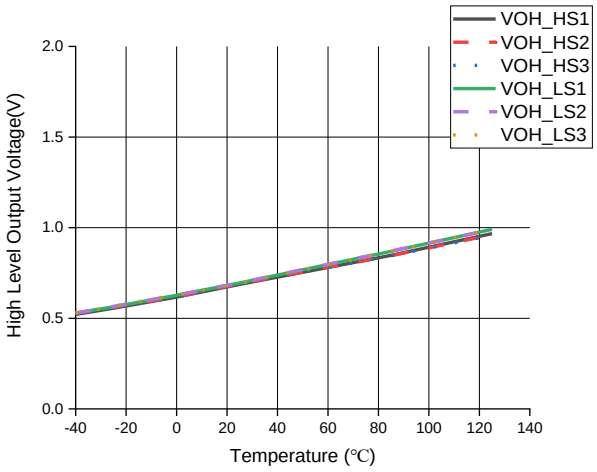
Logic "1" Input Threshold vs. Supply Voltage



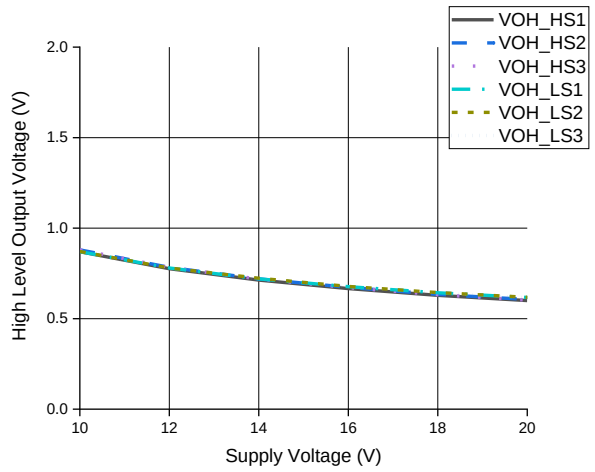
ITRIP Positive Going Threshold vs. Temperature



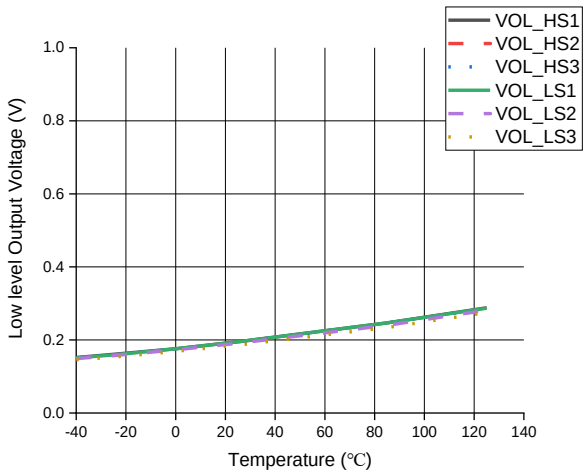
ITRIP Positive Going Threshold vs. Supply Voltage



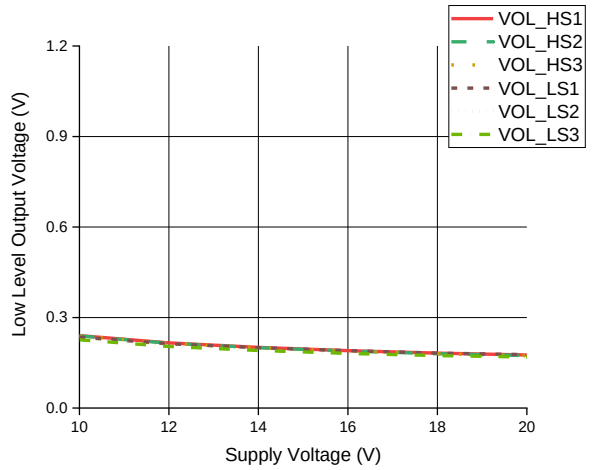
Output High Voltage vs. Temperature



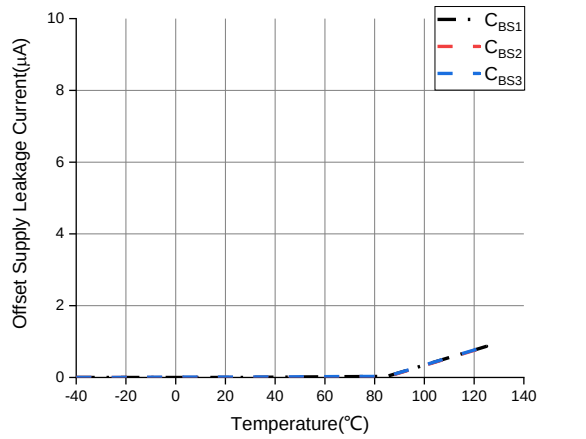
Output High Voltage vs. Supply Voltage



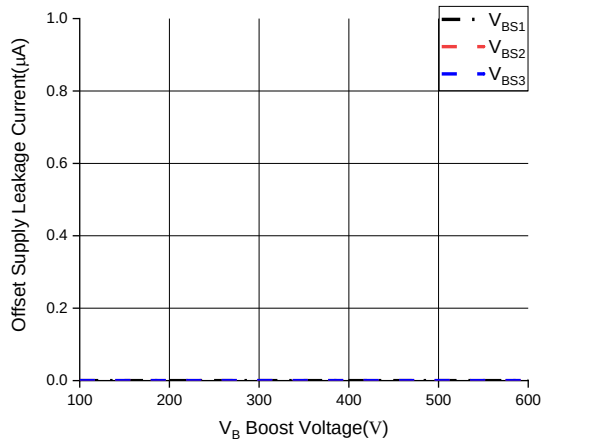
Output Low Voltage vs. Temperature



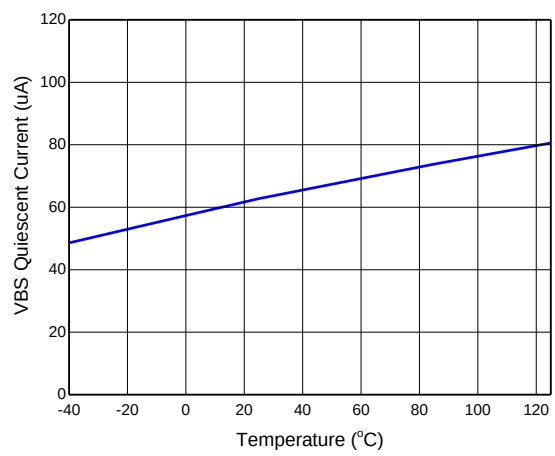
Output Low Voltage vs. Supply Voltage



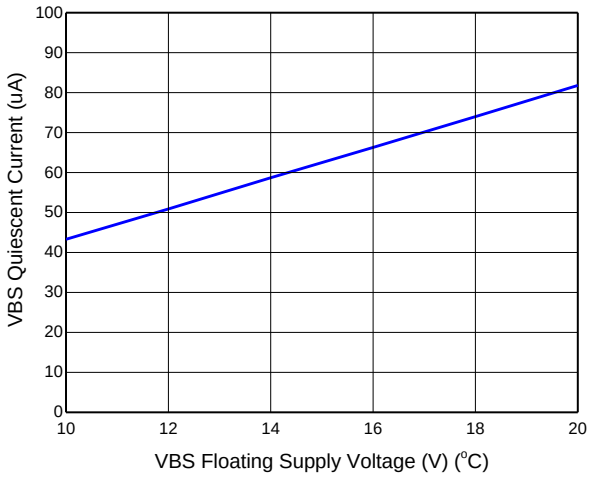
Offset Supply Leakage Current vs. V_B Temperature



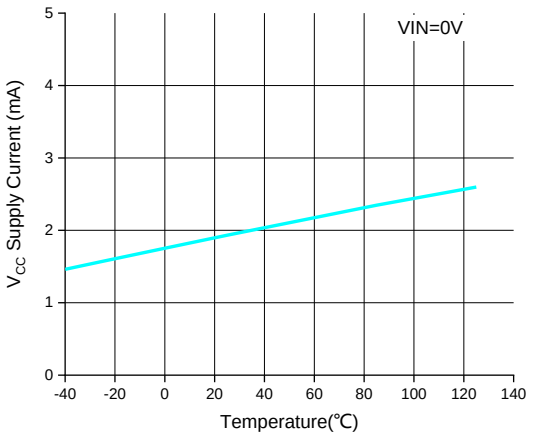
Offset Supply Leakage Current vs. V_B Boost Voltage



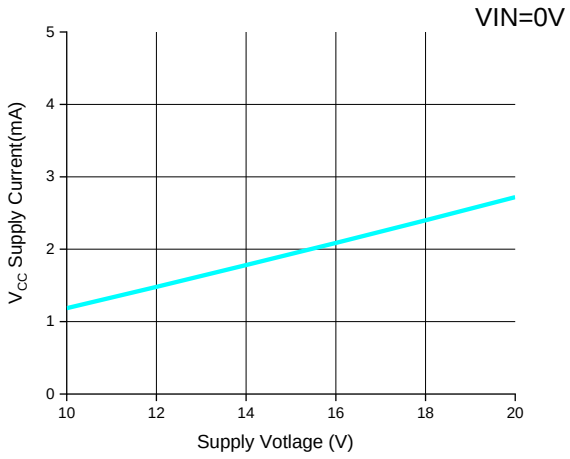
V_{BS} Supply Current vs. Temperature



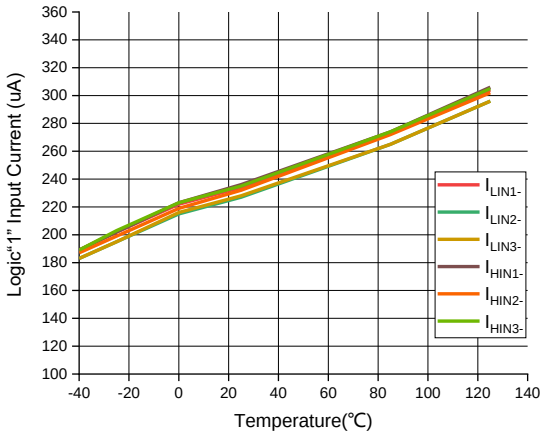
V_{BS} Supply Current vs. Supply Voltage



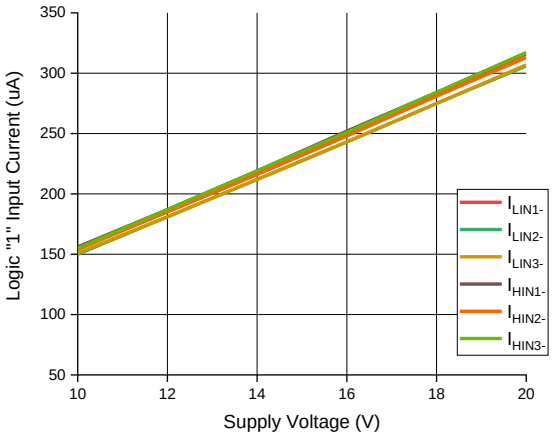
V_{CC} Supply Current vs. Temperature



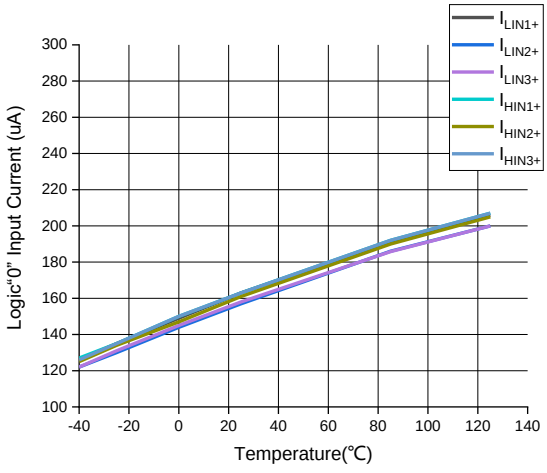
V_{CC} Supply Current vs. Supply Voltage



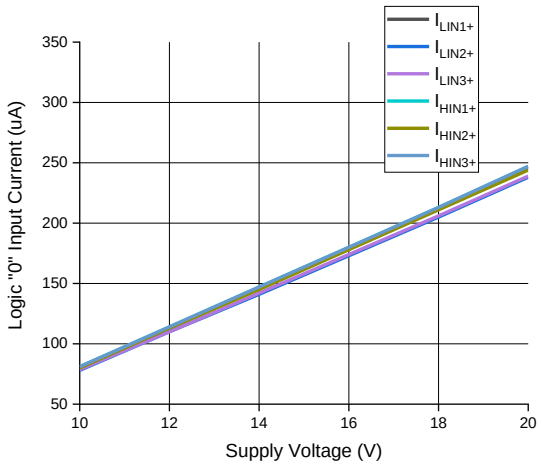
Logic "1" Input Current vs. Temperature



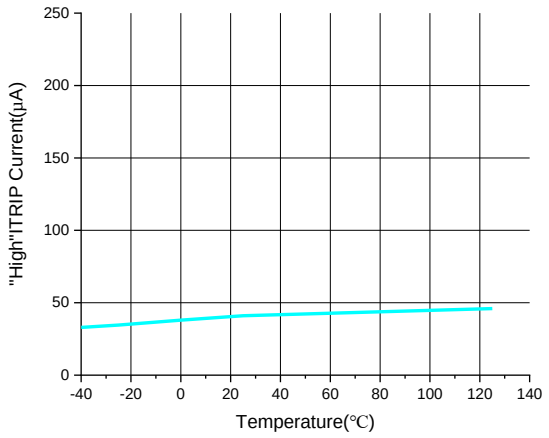
Logic "1" Input Current vs. Supply Voltage



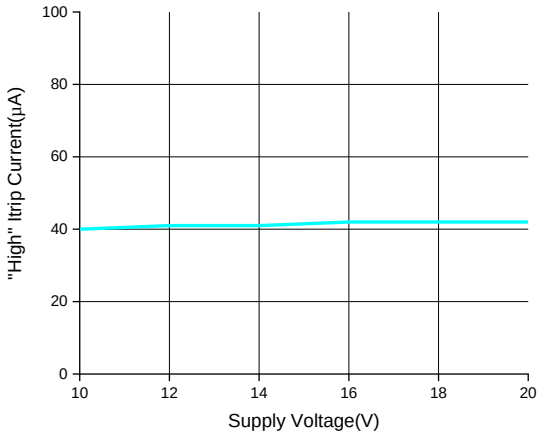
Logic "0" Input Current vs. Temperature



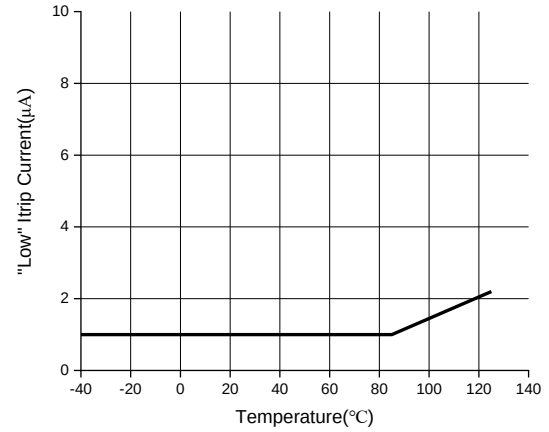
Logic "0" Input Current vs. Supply Voltage



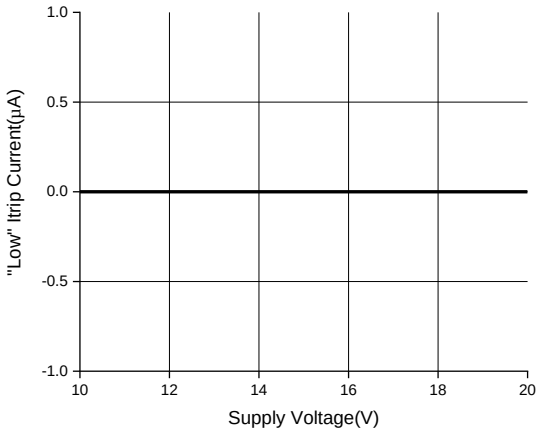
"High" ITRIP Current vs. Temperature



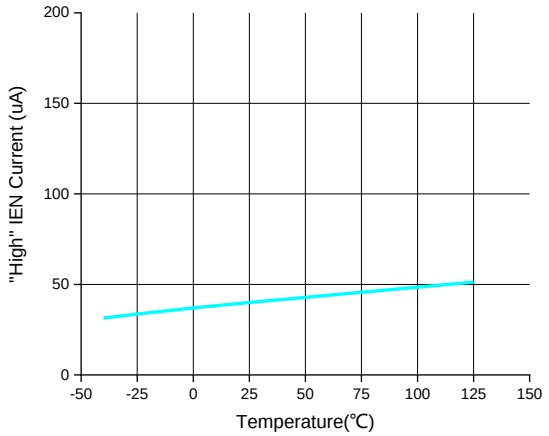
"High" ITRIP Current vs. Supply Voltage



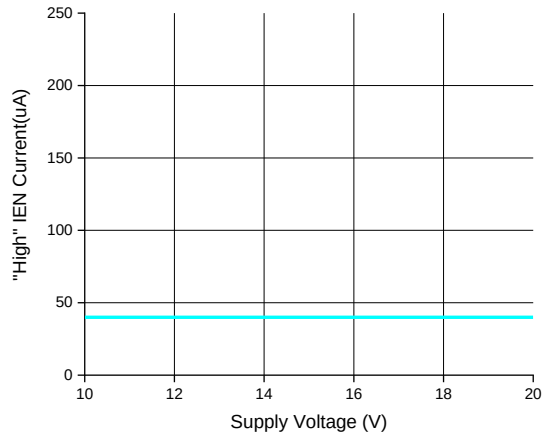
"Low" ITRIP Current vs. Temperature



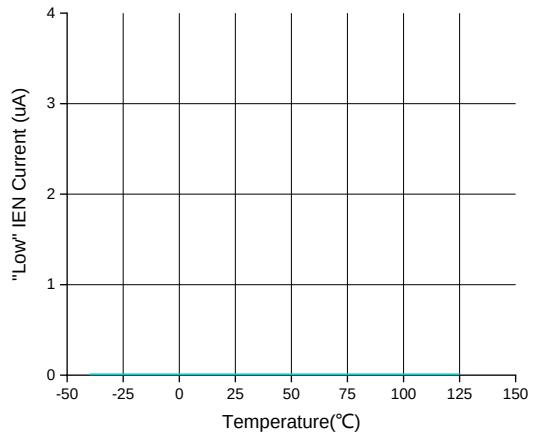
"Low" ITRIP Current vs. Voltage



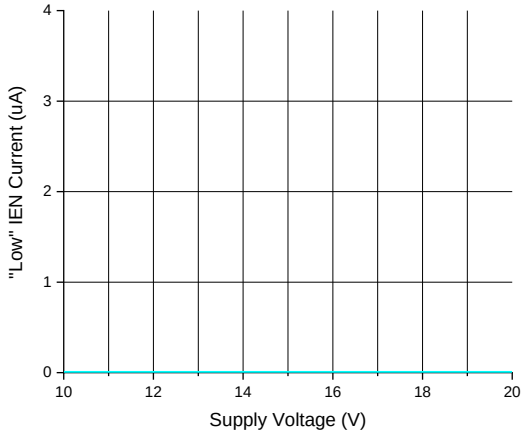
"High" IEN Current vs. Temperature



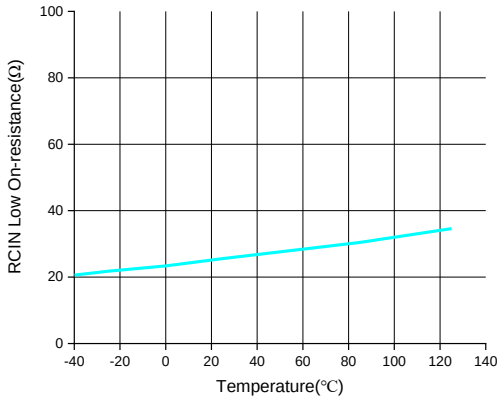
"High" IEN Current Vs Supply Voltage



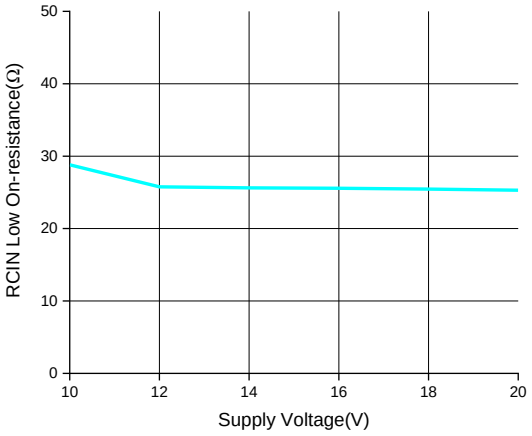
"Low" IEN Current Vs Temperature



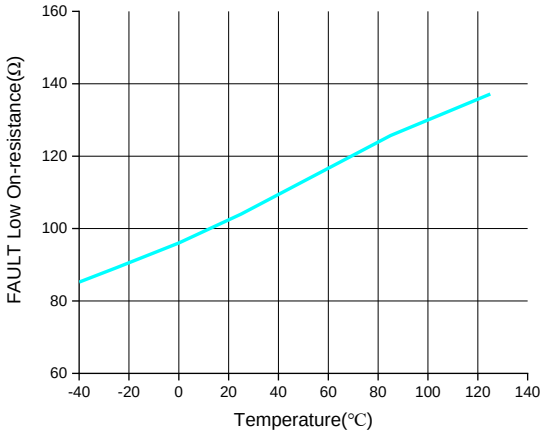
"Low" IEN current vs Supply Voltage



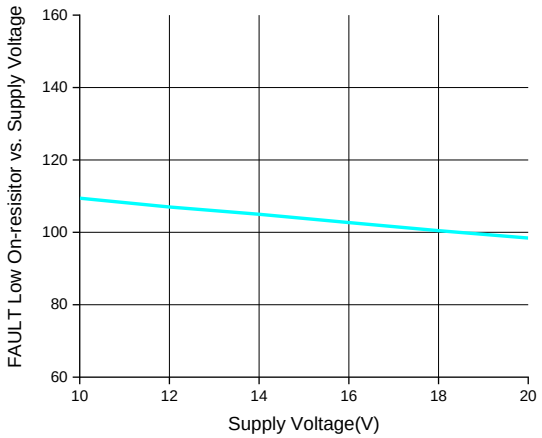
RCIN Low On-resistance vs. Temperature



RCIN Low On-resistance vs. Supply Voltage

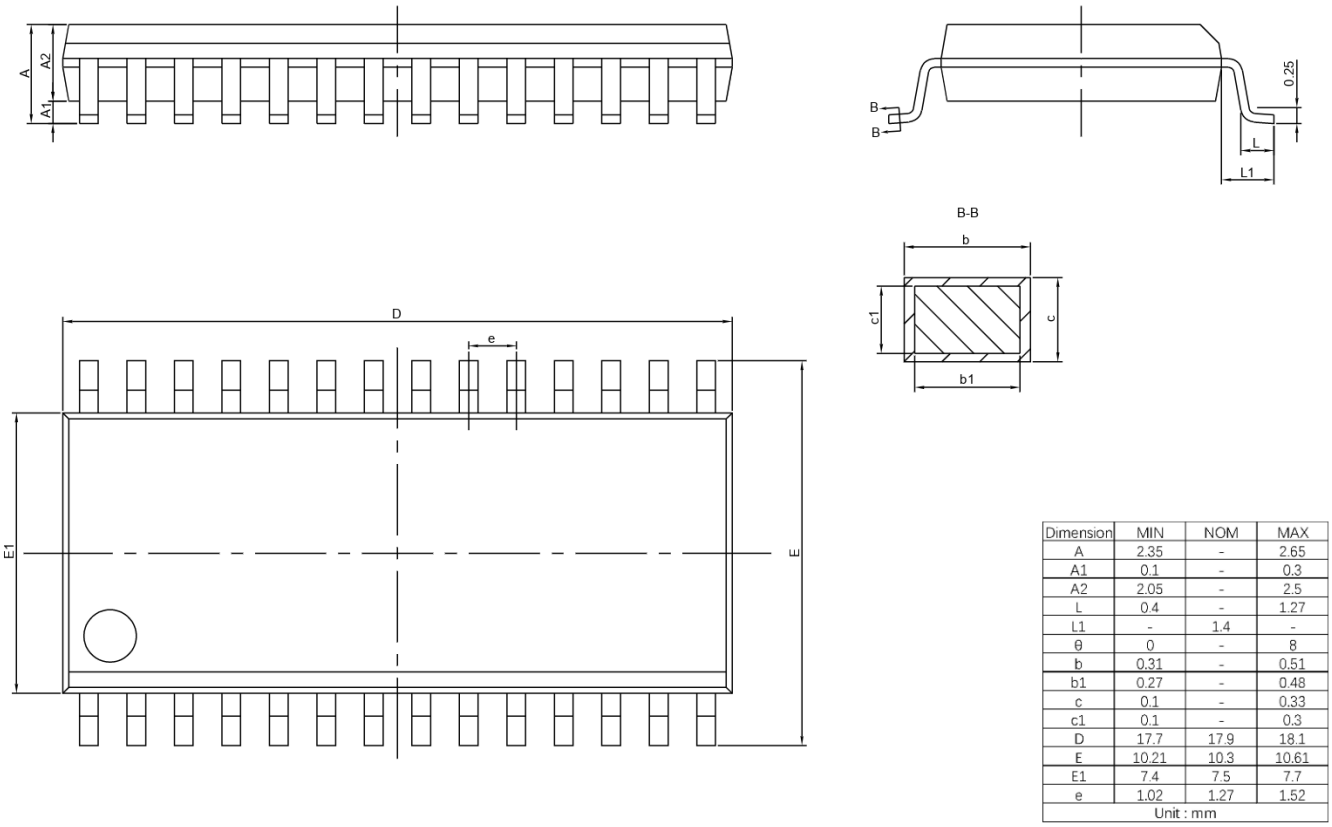


FAULT Low On-resistance vs. Temperature



FAULT Low On-resistance vs. Supply Voltage

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	2.35	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.5
L	0.4	-	1.27
L1	-	1.4	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	17.7	17.9	18.1
E	10.21	10.3	10.61
E1	7.4	7.5	7.7
e	1.02	1.27	1.52
Unit : mm			

Figure 7. SOP28W Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “Figure1” and “June 2019”
Page 6	Revise $V_{RCIN,HYS}$ parameter
Rev 1.1 datasheet, 2019-11-27	
Page 1	Remove a typo
Page 2	Change order information
Rev 1.2 datasheet, 2020-10-15	
Page 3	Block diagram modified
Page 10-Page 19	Update characteristic chart
Rev 1.3 datasheet, 2022-8-2	
Whole datasheet	Update the logo and format
Page 6, 7,8	Update t_{on}, t_{off}, t_{ITRIP}, t_{FLT}, t_{FILIN}, t_{FLTCLR}, DT, MT in the dynamic electrical characteristics Update V_{IH}, V_{IL}, $V_{IT,TH+}$, V_{IN_CLAMP}, I_{IN+}, I_{IN-}, I_{ITRIP+}, I_{EN+}, R_{on_FAULT} in the static electrical characteristic.
Page 21	Change the package name from SOIC28 to SOP28W